**K4A8G045WC**
**K4A8G085WC**

# 8Gb C-die DDR4 SDRAM

78FBGA with Lead-Free & Halogen-Free
(RoHS compliant)

1.2V

datasheet

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# Table Of Contents

## 8Gb C-die DDR4 SDRAM

1. Ordering Information ..... 5
2. Key Features ..... 5
3. Package Pinout/Mechanical Dimension & Addressing ..... 6
3.1 x4 Package Pinout (Top view): 78ball FBGA Package ..... 6
3.2 x8 Package Pinout (Top view) : 78ball FBGA Package ..... 7
3.3 FBGA Package Dimension (x4/x8) ..... 8
4. Input/Output Functional Description ..... 9
5. DDR4 SDRAM Addressing ..... 11
6. Absolute Maximum Ratings ..... 12
6.1 Absolute Maximum DC Ratings ..... 12
6.2 DRAM Component Operating Temperature Range ..... 12
7. AC & DC Operating Conditions ..... 12
8. AC & DC Input Measurement Levels ..... 13
8.1 AC & DC Logic Input Levels for Single-ended Signals ..... 13
8.2 VREF Tolerances ..... 13
8.3 AC & DC Logic Input Levels for Differential Signals ..... 14
8.3.1. Differential Signals Definition ..... 14
8.3.2. Differential Swing Requirement for Clock (CK_t - CK_c) ..... 14
8.3.3. Single-ended Requirements for Differential Signals ..... 15
8.3.4. Address, Command and Control Overshoot and Undershoot Specifications ..... 16
8.3.5. Clock Overshoot and Undershoot Specifications ..... 17
8.3.6. Data, Strobe and Mask Overshoot and Undershoot Specifications ..... 18
8.4 Slew Rate Definitions ..... 19
8.4.1. Slew Rate Definitions for Differential Input Signals (CK) ..... 19
8.4.2. Slew Rate Definition for Single-ended Input Signals ( CMD/ADD ) ..... 20
8.5 Differential Input Cross Point Voltage ..... 21
8.6 CMOS Rail to Rail Input Levels ..... 22
8.6.1. CMOS Rail to Rail Input Levels for RESET_n ..... 22
8.7 AC and DC Logic Input Levels for DQS Signals ..... 23
8.7.1. Differential Signal Definition ..... 23
8.7.2. Differential Swing Requirements for DQS (DQS_t - DQS_c) ..... 23
8.7.3. Peak Voltage Calculation Method ..... 24
8.7.4. Differential Input Cross Point Voltage ..... 25
8.7.5. Differential Input Slew Rate Definition ..... 26
9. AC and DC Output Measurement Levels ..... 27
9.1 Output Driver DC Electrical Characteristics ..... 27
9.1.1. Alert_n Output Drive Characteristic ..... 29
9.1.2. Output Driver Characteristic of Connectivity Test ( CT ) Mode ..... 29
9.2 Single-ended AC & DC Output Levels ..... 30
9.3 Differential AC & DC Output Levels ..... 30
9.4 Single-ended Output Slew Rate ..... 31
9.5 Differential Output Slew Rate ..... 32
9.6 Single-ended AC & DC Output Levels of Connectivity Test Mode ..... 33
9.7 Test Load for Connectivity Test Mode Timing ..... 33
10. Speed Bin ..... 34
10.1 Speed Bin Table Note ..... 39
11. IDD and IDDQ Specification Parameters and Test Conditions ..... 40
11.1 IDD, IPP and IDDQ Measurement Conditions ..... 40
12. 8Gb DDR4 SDRAM C-die IDD Specification Table ..... 55
13. Input/Output Capacitance ..... 57
14. Electrical Characteristics & AC Timing ..... 59
14.1 Reference Load for AC Timing and Output Slew Rate ..... 59
14.2 tREFI ..... 59

14.3 Clock Specification ..... 60
14.3.1. Definition for tCK(abs) ..... 60
14.3.2. Definition for tCK(avg) ..... 60
14.3.3. Definition for tCH(avg) and tCL(avg) ..... 60
14.3.4. Definition for tERR(nper) ..... 60
14.4 Timing Parameters by Speed Grade ..... 61
14.5 Rounding Algorithms ..... 67
14.6 The DQ Input Receiver Compliance Mask for Voltage and Timing ..... 68
14.7 DDR4 Function Matrix ..... 72

# 1. Ordering Information

**[ Table 1 ] Samsung 8Gb DDR4 C-die Ordering Information Table**

| Organization | DDR4-2133 (15-15-15) | DDR4-2400 (17-17-17)[2] | DDR4-2666(19-19-19)[2] | Package |
|---|---|---|---|---|
| 2Gx4 | K4A8G045WC-BCPB | K4A8G045WC-BCRC | K4A8G045WC-BCTD | 78 FBGA |
| 1Gx8 | K4A8G085WC-BCPB | K4A8G085WC-BCRC | K4A8G085WC-BCTD | 78 FBGA |

**NOTE** :
1. Speed bin is in order of CL-tRCD-tRP.
2. Backward compatible to lower frequency

# 2. Key Features

**[ Table 2 ] 8Gb DDR4 C-die Speed Bins**

| Speed | DDR4-1600 | DDR4-1866 | DDR4-2133 | DDR4-2400 | DDR4-2666 | Unit |
|---|---|---|---|---|---|---|
| | 11-11-11 | 13-13-13 | 15-15-15 | 17-17-17 | 19-19-19 | |
| tCK(min) | 1.25 | 1.071 | 0.937 | 0.833 | 0.75 | ns |
| CAS Latency | 11 | 13 | 15 | 17 | 19 | nCK |
| tRCD(min) | 13.75 | 13.92 | 14.06 | 14.16 | 14.25 | ns |
| tRP(min) | 13.75 | 13.92 | 14.06 | 14.16 | 14.25 | ns |
| tRAS(min) | 35 | 34 | 33 | 32 | 32 | ns |
| tRC(min) | 48.75 | 47.92 | 47.06 | 46.16 | 46.25 | ns |

- JEDEC standard 1.2V (1.14V~1.26V)
- $V_{DDQ}$ = 1.2V (1.14V~1.26V)
- 800 MHz $f_{CK}$ for 1600Mb/sec/pin, 933 MHz $f_{CK}$ for 1866Mb/sec/pin, 1067MHz $f_{CK}$ for 2133Mb/sec/pin, 1200MHz $f_{CK}$ for 2400Mb/sec/pin, 1333MHz $f_{CK}$ for 2666Mb/sec/pin
- 16 Banks (4 Bank Groups)
- Programmable CAS Latency (posted CAS): 10,11,12,13,14,15,16,17,18,19,20
- Programmable Additive Latency: 0, CL-2 or CL-1 clock
- Programmable CAS Write Latency (CWL) = 9,11 (DDR4-1600), 10,12 (DDR4-1866),11,14 (DDR4-2133),12,16 (DDR4-2400) and 14,18 (DDR4-2666)
- 8-bit pre-fetch
- Burst Length: 8, 4 with tCCD = 4 which does not allow seamless read or write [either On the fly using A12 or MRS]
- Bi-directional Differential Data-Strobe
- Internal (self) calibration: Internal self calibration through ZQ pin (RZQ: 240 ohm ± 1%)
- On Die Termination using ODT pin
- Average Refresh Period 7.8us at lower than $T_{CASE}$ 85°C, 3.9us at 85°C < $T_{CASE} \leq$ 95 °C
- Connectivity Test Mode (TEN) is Supported
- Asynchronous Reset
- Package: 78 balls FBGA - x4/x8
- All of Lead-Free products are compliant for RoHS
- All of products are Halogen-free
- CRC (Cyclic Redundancy Check) for Read/Write data security
- Command address parity check
- DBI (Data Bus Inversion)
- Gear down mode
- POD (Pseudo Open Drain) interface for data input/output
- Internal VREF for data inputs
- External VPP for DRAM Activating Power
- PPR and sPPR is supported

The 8Gb DDR4 SDRAM C-die is organized as a 128Mbit x 4 I/Os x 16banks or 64Mbit x8 I/Os x 16banks device. This synchronous device achieves high speed double-data-rate transfer rates of up to 2666Mb/sec/pin (DDR4-2666) for general applications.

The chip is designed to comply with the following key DDR4 SDRAM features such as posted CAS, Programmable CWL, Internal (Self) Calibration, On Die Termination using ODT pin and Asynchronous Reset.

All of the control and address inputs are synchronized with a pair of externally supplied differential clocks. Inputs are latched at the crosspoint of differential clocks (CK rising and $\overline{CK}$ falling). All I/Os are synchronized with a pair of bidirectional strobes (DQS and $\overline{DQS}$) in a source synchronous fashion. The address bus is used to convey row, column, and bank address information in a $\overline{RAS}/\overline{CAS}$ multiplexing style. The DDR4 device operates with a single 1.2V (1.14V~1.26V) power supply and 1.2V (1.14V~1.26V).
The 8Gb DDR4 C-die device is available in 78ball FBGAs(x4/x8).

**NOTE**:
1. This data sheet is an abstract of full DDR4 specification and does not cover the common features which are described in “DDR4 SDRAM Device Operation & Timing Diagram”.
2. The functionality described and the timing specifications included in this data sheet are for the DLL Enabled mode of operation.

# 3. Package Pinout/Mechanical Dimension & Addressing

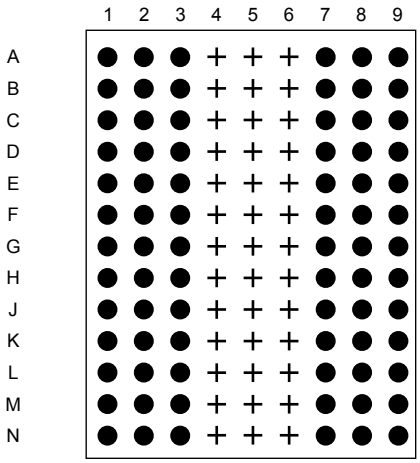
## 3.1 x4 Package Pinout (Top view): 78ball FBGA Package

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | |
|---|---|---|---|---|---|---|---|---|---|---|
| A | VDD | VSSQ | NC | | | | NC | VSSQ | VSS | A |
| B | VPP | VDDQ | DQS_c | | | | DQ1 | VDDQ | ZQ | B |
| C | VDDQ | DQ0 | DQS_t | | | | VDD | VSS | VDDQ | C |
| D | VSSQ | NC | DQ2 | | | | DQ3 | NC | VSSQ | D |
| E | VSS | VDDQ | NC | | | | NC | VDDQ | VSS | E |
| F | VDD | NC | ODT | | | | CK_t | CK_c | VDD | F |
| G | VSS | NC | CKE | | | | CS_n | NC | TEN | G |
| H | VDD | WE_n A14 | ACT_n | | | | CAS_n A15 | RAS_n A16 | VSS | H |
| J | VREFCA | BG0 | A10 AP | | | | A12 BC_n | BG1 | VDD | J |
| K | VSS | BA0 | A4 | | | | A3 | BA1 | VSS | K |
| L | RESET_n | A6 | A0 | | | | A1 | A5 | ALERT_n | L |
| M | VDD | A8 | A2 | | | | A9 | A7 | VPP | M |
| N | VSS | A11 | PAR | | | | NC | A13 | VDD | N |

**Ball Locations (x4)**

● **Populated ball**
\+ **Ball not populated**

**Top view**
(See the balls through the package)



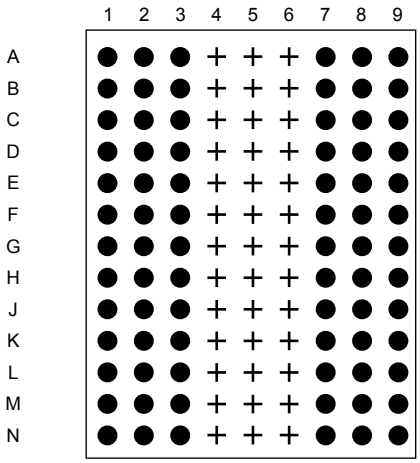
## 3.2 x8 Package Pinout (Top view) : 78ball FBGA Package

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | |
|---|---|---|---|---|---|---|---|---|---|---|
| A | VDD | VSSQ | TDQS_c | | | | DM_n, DBI_n, TDQS_t | VSSQ | VSS | A |
| B | VPP | VDDQ | DQS_c | | | | DQ1 | VDDQ | ZQ | B |
| C | VDDQ | DQ0 | DQS_t | | | | VDD | VSS | VDDQ | C |
| D | VSSQ | DQ4 | DQ2 | | | | DQ3 | DQ5 | VSSQ | D |
| E | VSS | VDDQ | DQ6 | | | | DQ7 | VDDQ | VSS | E |
| F | VDD | NC | ODT | | | | CK_t | CK_c | VDD | F |
| G | VSS | NC | CKE | | | | CS_n | NC | TEN | G |
| H | VDD | WE_n A14 | ACT_n | | | | CAS_n A15 | RAS_n | VSS | H |
| J | VREFCA | BG0 | A10 AP | | | | A12 BC_n | BG1 | VDD | J |
| K | VSS | BA0 | A4 | | | | A3 | BA1 | VSS | K |
| L | RESET_n | A6 | A0 | | | | A1 | A5 | ALERT_n | L |
| M | VDD | A8 | A2 | | | | A9 | A7 | VPP | M |
| N | VSS | A11 | PAR | | | | NC | A13 | VDD | N |

### Ball Locations (x8)

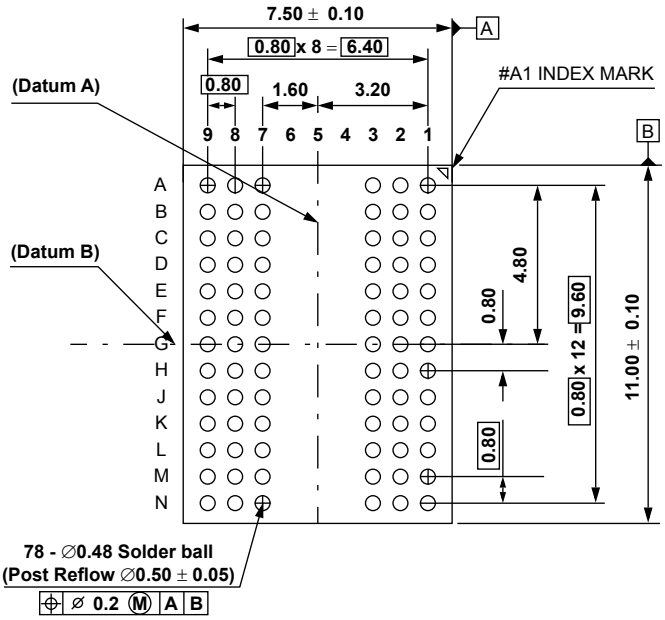
● **Populated ball**
\+ **Ball not populated**

**Top view**
(See the balls through the package)

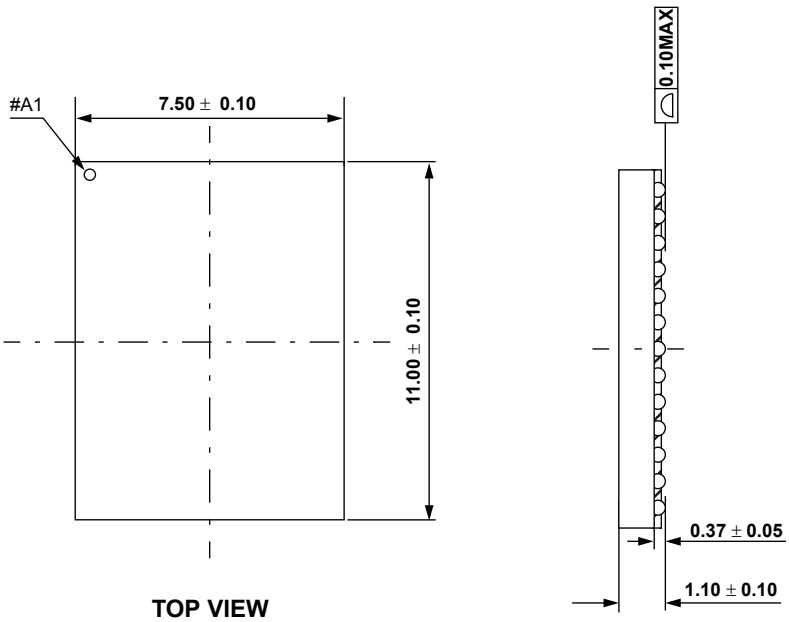


## 3.3 FBGA Package Dimension (x4/x8)

Units : Millimeters




**BOTTOM VIEW**




**TOP VIEW**

# 4. Input/Output Functional Description

**[ Table 3 ] Input/Output Function Description**

| Symbol | Type | Function |
|---|---|---|
| CK_t, CK_c | Input | Clock: CK_t and CK_c are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK_t and negative edge of CK_c. |
| CKE, (CKE1) | Input | Clock Enable: CKE HIGH activates, and CKE Low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE Low provides Precharge Power-Down and Self-Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is synchronous for Self-Refresh exit. After VREFCA and Internal DQ Vref have become stable during the power on and initialization sequence, they must be maintained during all operations (including Self-Refresh). CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK_t,CK_c, ODT and CKE are disabled during power-down. Input buffers, excluding CKE, are disabled during Self-Refresh. |
| CS_n, (CS1_n) | Input | Chip Select: All commands are masked when CS_n is registered HIGH. CS_n provides for external Rank selection on systems with multiple Ranks. CS_n is considered part of the command code. |
| C0,C1,C2 | Input | Chip ID : Chip ID is only used for 3DS for 2,4,8high stack via TSV to select each slice of stacked component. Chip ID is considered part of the command code |
| ODT, (ODT1) | Input | On Die Termination: ODT (registered HIGH) enables RTT_NOM termination resistance internal to the DDR4 SDRAM. When enabled, ODT is only applied to each DQ, DQS_t, DQS_c and DM_n/DBI_n/ TDQS_t, NU/TDQS_c (When TDQS is enabled via Mode Register A11=1 in MR1) signal for x8 conurations. For x16 conuration ODT is applied to each DQ, DQSU_t, DQSU_c, DQSL_t, DQSL_c, DMU_n, and DML_n signal. The ODT pin will be ignored if MR1 is programmed to disable RTT_NOM. |
| ACT_n | Input | Activation Command Input : ACT_n defines the Activation command being entered along with CS_n. The input into RAS_n/A16, CAS_n/A15 and WE_n/A14 will be considered as Row Address A16, A15 and A14 |
| RAS_n/A16. CAS_n/ A15. WE_n/A14 | Input | Command Inputs: RAS_n/A16, CAS_n/A15 and WE_n/A14 (along with CS_n) define the command being entered. Those pins have multi function. For example, for activation with ACT_n Low, those are Addressing like A16,A15 and A14 but for non-activation command with ACT_n High, those are Command pins for Read, Write and other command defined in command truth table |
| DM_n/DBI_n/TDQS_t, (DMU_n/DBIU_n), (DML_n/DBIL_n) | Input/Output | Input Data Mask and Data Bus Inversion: DM_n is an input mask signal for write data. Input data is masked when DM_n is sampled LOW coincident with that input data during a Write access. DM_n is sampled on both edges of DQS. DM is muxed with DBI function by Mode Register A10,A11,A12 setting in MR5. For x8 device, the function of DM or TDQS is enabled by Mode Register A11 setting in MR1. DBI_n is an input/output identifing whether to store/output the true or inverted data. If DBI_n is LOW, the data will be stored/output after inversion inside the DDR4 SDRAM and not inverted if DBI_n is HIGH. TDQS is only supported in X8 |
| BG0 - BG1 | Input | Bank Group Inputs : BG0 - BG1 define to which bank group an Active, Read, Write or Precharge command is being applied. BG0 also determines which mode register is to be accessed during a MRS cycle. X4/8 have BG0 and BG1 but X16 has only BG0 |
| BA0 - BA1 | Input | Bank Address Inputs: BA0 - BA1 define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines which mode register is to be accessed during a MRS cycle. |
| A0 - A17 | Input | Address Inputs: Provide the row address for ACTIVATE Commands and the column address for Read/ Write commands to select one location out of the memory array in the respective bank. (A10/AP, A12/ BC_n, RAS_n/A16, CAS_n/A15 and WE_n/A14 have additional functions, see other rows.The address inputs also provide the op-code during Mode Register Set commands.A17 is only defined for the x4 conuration. |
| A10 / AP | Input | Auto-precharge: A10 is sampled during Read/Write commands to determine whether Autoprecharge should be performed to the accessed bank after the Read/Write operation. (HIGH: Autoprecharge; LOW: no Autoprecharge).A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by bank addresses. |
| A12 / BC_n | Input | Burst Chop: A12 / BC_n is sampled during Read and Write commands to determine if burst chop (on-the-fly) will be performed. (HIGH, no burst chop; LOW: burst chopped). See command truth table for details. |
| RESET_n | Input | Active Low Asynchronous Reset: Reset is active when RESET_n is LOW, and inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation. RESET_n is a CMOS rail to rail signal with DC high and low at 80% and 20% of $V_{DD}$, |
| DQ | Input / Output | Data Input/ Output: Bi-directional data bus. If CRC is enabled via Mode register then CRC code is added at the end of Data Burst. Any DQ from DQ0~DQ3 may indicate the internal Vref level during test via Mode Register Setting MR4 A4=High. During this mode, RTT value should be set to Hi-Z. Refer to vendor specific datasheets to determine which DQ is used. |
| DQS_t, DQS_c, DQSU_t, DQSU_c, DQSL_t, DQSL_c | Input / Output | Data Strobe: output with read data, input with write data. Edge-aligned with read data, centered in write data. For the x16, DQSL corresponds to the data on DQL0-DQL7; DQSU corresponds to the data on DQU0-DQU7. The data strobe DQS_t, DQSL_t and DQSU_t are paired with differential signals DQS_c, DQSL_c, and DQSU_c, respectively, to provide differential pair signaling to the system during reads and writes. DDR4 SDRAM supports differential data strobe only and does not support single-ended. |

| Symbol | Type | Function |
|---|---|---|
| TDQS_t, TDQS_c | Output | Termination Data Strobe: TDQS_t/TDQS_c is applicable for x8 DRAMs only. When enabled via Mode Register A11 = 1 in MR1, the DRAM will enable the same termination resistance function on TDQS_t/TDQS_c that is applied to DQS_t/DQS_c. When disabled via mode register A11 = 0 in MR1, DM/DBI/TDQS will provide the data mask function or Data Bus Inversion depending on MR5; A11,12,10and TDQS_c is not used. x4/x16 DRAMs must disable the TDQS function via mode register A11 = 0 in MR1. |
| PAR | Input | Command and Address Parity Input : DDR4 Supports Even Parity check in DRAM with MR setting. Once it's enabled via Register in MR5, then DRAM calculates Parity with ACT_n,RAS_n/A16,CAS_n/A15,WE_n/A14,BG0-BG1,BA0-BA1,A17-A0, and C0-C2 (3DS devices). Input parity should maintain at the rising edge of the clock and at the same time with command & address with CS_n LOW |
| ALERT_n | Input/Output | Alert : It has multi functions such as CRC error flag , Command and Address Parity error flag as Output signal. If there is error in CRC, then Alert_n goes LOW for the period time interval and goes back HIGH. If there is error in Command Address Parity Check, then Alert_n goes LOW for relatively long period until on going DRAM internal recovery transaction to complete. During Connectivity Test mode, this pin works as input. Using this signal or not is dependent on system. In case of not connected as Signal, ALERT_n Pin must be bounded to VDD on board. |
| TEN | Input | Connectivity Test Mode Enable : Required on X16 devices and optional input on x4/x8 with densities equal to or greater than 8Gb.HIGH in this pin will enable Connectivity Test Mode operation along with other pins. It is a CMOS rail to rail signal with AC high and low at 80% and 20% of VDD. Using this signal or not is dependent on System. This pin may be DRAM internally pulled low through a weak pull-down resistor to VSS. |
| NC | | No Connect: No internal electrical connection is present. |
| VDDQ | Supply | DQ Power Supply: 1.2 V +/- 0.06 V |
| VSSQ | Supply | DQ Ground |
| VDD | Supply | Power Supply: 1.2 V +/- 0.06 V |
| VSS | Supply | Ground |
| VPP | Supply | DRAM Activating Power Supply: 2.5V ( 2.375V min , 2.75V max) |
| VREFCA | Supply | Reference voltage for CA |
| ZQ | Supply | Reference Pin for ZQ calibration |
| NOTE Input only pins (BG0-BG1,BA0-BA1, A0-A17, ACT_n, RAS_n/A16, CAS_n/A15, WE_n/A14, CS_n, CKE, ODT, and RESET_n) do not supply termination. | | |

# 5. DDR4 SDRAM Addressing

## 2 Gb Addressing Table

| Configuration | | 512 Mb x4 | 256 Mb x8 | 128 Mb x16 |
|---|---|---|---|---|
| Bank Address | # of Bank Groups | 4 | 4 | 2 |
| | BG Address | BG0~BG1 | BG0~BG1 | BG0 |
| | Bank Address in a BG | BA0~BA1 | BA0~BA1 | BA0~BA1 |
| Row Address | | A0~A14 | A0~A13 | A0~A13 |
| Column Address | | A0~A9 | A0~A9 | A0~A9 |
| Page size | | 512B | 1KB | 2KB |

## 4 Gb Addressing Table

| Configuration | | 1 Gb x4 | 512 Mb x8 | 256 Mb x16 |
|---|---|---|---|---|
| Bank Address | # of Bank Groups | 4 | 4 | 2 |
| | BG Address | BG0~BG1 | BG0~BG1 | BG0 |
| | Bank Address in a BG | BA0~BA1 | BA0~BA1 | BA0~BA1 |
| Row Address | | A0~A15 | A0~A14 | A0~A14 |
| Column Address | | A0~A9 | A0~A9 | A0~A9 |
| Page size | | 512B | 1KB | 2KB |

## 8 Gb Addressing Table

| Configuration | | 2 Gb x4 | 1 Gb x8 | 512 Mb x16 |
|---|---|---|---|---|
| Bank Address | # of Bank Groups | 4 | 4 | 2 |
| | BG Address | BG0~BG1 | BG0~BG1 | BG0 |
| | Bank Address in a BG | BA0~BA1 | BA0~BA1 | BA0~BA1 |
| Row Address | | A0~A16 | A0~A15 | A0~A15 |
| Column Address | | A0~A9 | A0~A9 | A0~A9 |
| Page size | | 512B | 1KB | 2KB |

## 16 Gb Addressing Table

| Configuration | | 4 Gb x4 | 2 Gb x8 | 1 Gb x16 |
|---|---|---|---|---|
| Bank Address | # of Bank Groups | 4 | 4 | 2 |
| | BG Address | BG0~BG1 | BG0~BG1 | BG0 |
| | Bank Address in a BG | BA0~BA1 | BA0~BA1 | BA0~BA1 |
| Row Address | | A0~A17 | A0~A16 | A0~A16 |
| Column Address | | A0~A9 | A0~A9 | A0~A9 |
| Page size | | 512B | 1KB | 2KB |

**NOTE** 1 : Page size is the number of bytes of data delivered from the array to the internal sense amplifiers when an ACTIVE command is registered.
Page size is per bank, calculated as follows: page size = $2^{COLBITS} * ORG \div 8$
where, COLBITS = the number of column address bits, ORG = the number of I/O (DQ) bits

# 6. Absolute Maximum Ratings

## 6.1 Absolute Maximum DC Ratings

**[ Table 4 ] Absolute Maximum DC Ratings**

| Symbol | Parameter | Rating | Units | NOTE |
|---|---|---|---|---|
| VDD | Voltage on VDD pin relative to Vss | -0.3 ~ 1.5 | V | 1,3 |
| VDDQ | Voltage on VDDQ pin relative to Vss | -0.3 ~ 1.5 | V | 1,3 |
| VPP | Voltage on VPP pin relative to Vss | -0.3 ~ 3.0 | V | 4 |
| $V_{IN}$, $V_{OUT}$ | Voltage on any pin except VREFCA relative to Vss | -0.3 ~ 1.5 | V | 1,3,5 |
| $T_{STG}$ | Storage Temperature | -55 to +100 | °C | 1,2 |

**NOTE :**

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability
2. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
3. VDD and VDDQ must be within 300 mV of each other at all times;and VREFCA must be not greater than 0.6 x VDDQ, When VDD and VDDQ are less than 500 mV; VREFCA may be equal to or less than 300 mV
4. VPP must be equal or greater than VDD/VDDQ at all times.
5. Overshoot area above 1.5 V is specified in section 8.3.4, 8.3.5 and section 8.3.6.

## 6.2 DRAM Component Operating Temperature Range

**[ Table 5 ] Temperature Range**

| Symbol | Parameter | rating | Unit | NOTE |
|---|---|---|---|---|
| $T_{OPER}$ | Operating Temperature Range | 0 to 95 | °C | 1, 2, 3 |

**NOTE** :

1. Operating Temperature $T_{OPER}$ is the case surface temperature on the center/top side of the DRAM.
2. The Normal Temperature Range specifies the temperatures where all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0-85°C under all operating conditions
3. Some applications require operation of the Extended Temperature Range between 85°C and 95°C case temperature. Full specifications are guaranteed in this range, but the following additional conditions apply:
   a) Refresh commands must be doubled in frequency, therefore reducing the refresh interval tREFI to 3.9us.
   b) If Self-Refresh operation is required in the Extended Temperature Range, then it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 A6 = $0_b$ and MR2 A7 = $1_b$), in this case IDD6 current can be increased around 10~20% than normal Temperature range.

# 7. AC & DC Operating Conditions

**[ Table 6 ] Recommended DC Operating Conditions**

| Symbol | Parameter | Rating | | | Unit | NOTE |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| VDD | Supply Voltage | 1.14 | 1.2 | 1.26 | V | 1,2,3 |
| VDDQ | Supply Voltage for Output | 1.14 | 1.2 | 1.26 | V | 1,2,3 |
| VPP | Peak-to-Peak Voltage | 2.375 | 2.5 | 2.75 | V | 3 |

**NOTE :**

1. Under all conditions VDDQ must be less than or equal to VDD.
2. VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together.
3. DC bandwidth is limited to 20MHz.

# 8. AC & DC Input Measurement Levels

## 8.1 AC & DC Logic Input Levels for Single-ended Signals

**[ Table 7 ] Single-ended AC & DC input Levels for Command and Address**

| Symbol | Parameter | DDR4-1600/1866/2133/2400 | | DDR4-2666 | | Unit | NOTE |
|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | | |
| $V_{IH.CA}$(DC75) | DC input logic high | $V_{REFCA}$+ 0.075 | $V_{DD}$ | TBD | TBD | V | |
| $V_{IL.CA}$(DC75) | DC input logic low | $V_{SS}$ | $V_{REFCA}$-0.075 | TBD | TBD | V | |
| $V_{IH.CA}$(AC100) | AC input logic high | $V_{REF}$ + 0.1 | Note 2 | TBD | TBD | V | 1 |
| $V_{IL.CA}$(AC100) | AC input logic low | Note 2 | $V_{REF}$ - 0.1 | TBD | TBD | V | 1 |
| $V_{REFCA}$(DC) | Reference Voltage for ADD, CMD inputs | 0.49*$V_{DD}$ | 0.51*$V_{DD}$ | TBD | TBD | V | 2,3 |

**NOTE** :
1. See “Overshoot and Undershoot Specifications” .
2. The AC peak noise on $V_{REFCA}$ may not allow $V_{REFCA}$ to deviate from $V_{REFCA}$(DC) by more than ± 1% $V_{DD}$ (for reference : approx. ± 12mV)
3. For reference : approx. $V_{DD}$/2 ± 12mV

## 8.2 $V_{REF}$ Tolerances

The DC-tolerance limits and ac-noise limits for the reference voltages $V_{REFCA}$ is illustrated in Figure 1. It shows a valid reference voltage $V_{REF}$(t) as a function of time. ($V_{REF}$ stands for $V_{REFCA}$ and $V_{REFDQ}$ likewise).

$V_{REF}$(DC) is the linear average of $V_{REF}$(t) over a very long period of time (e.g. 1 sec). This average has to meet the min/max requirement in Table 7. Furthermore $V_{REF}$(t) may temporarily deviate from $V_{REF}$(DC) by no more than ± 1% $V_{DD}$.

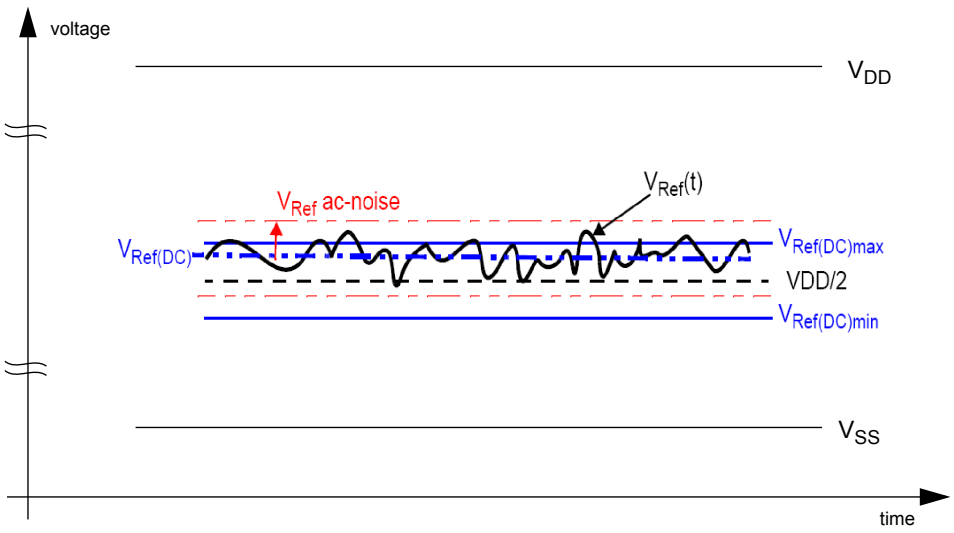



**Figure 1. Illustration of $V_{REF}$(DC) tolerance and VREF ac-noise limits**

The voltage levels for setup and hold time measurements $V_{IH}$(AC), $V_{IH}$(DC), $V_{IL}$(AC) and $V_{IL}$(DC) are dependent on $V_{REF}$.

"$V_{REF}$" shall be understood as $V_{REF}$(DC), as defined in Figure 1.

This clarifies, that DC-variations of $V_{REF}$ affect the absolute voltage a signal has to reach to achieve a valid high or low level and therefore the time to which setup and hold is measured. System timing and voltage budgets need to account for $V_{REF}$(DC) deviations from the optimum position within the data-eye of the input signals.

This also clarifies that the DRAM setup/hold specification and derating values need to include time and voltage associated with $V_{REF}$ ac-noise. Timing and voltage effects due to ac-noise on $V_{REF}$ up to the specified limit (+/-1% of $V_{DD}$) are included in DRAM timings and their associated deratings.

# 8.3 AC & DC Logic Input Levels for Differential Signals

## 8.3.1 Differential Signals Definition

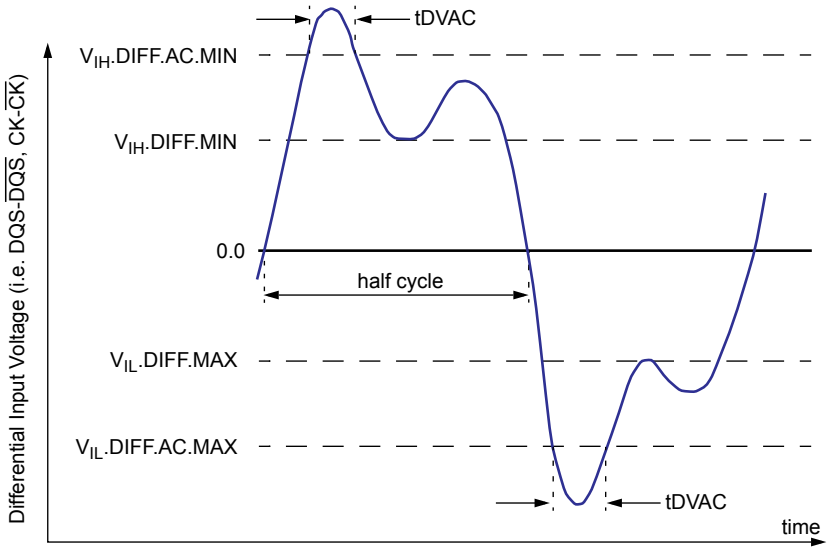



**Figure 2. Definition of differential ac-swing and "time above ac level" tDVAC**

**NOTE** :
1. Differential signal rising edge from VIL.DIFF.MAX to VIH.DIFF.MIN must be monotonic slope.
2. Differential signal falling edge from VIH.DIFF.MIN to VIL.DIFF.MAX must be monotonic slope.

## 8.3.2 Differential Swing Requirement for Clock (CK_t - CK_c)

**[ Table 8 ] Differential AC & DC Input Levels**

| Symbol | Parameter | DDR4 -1600/1866/2133 | | DDR4 -2400/2666 | | unit | NOTE |
|---|---|---|---|---|---|---|---|
| | | min | max | min | max | | |
| $V_{IHdiff}$ | differential input high | +0.150 | NOTE 3 | TBD | NOTE 3 | V | 1 |
| $V_{ILdiff}$ | differential input low | NOTE 3 | -0.150 | NOTE 3 | TBD | V | 1 |
| $V_{IHdiff}$(AC) | differential input high ac | 2 x ($V_{IH}$(AC) - $V_{REF}$) | NOTE 3 | 2 x ($V_{IH}$(AC) - $V_{REF}$) | NOTE 3 | V | 2 |
| $V_{ILdiff}$(AC) | differential input low ac | NOTE 3 | 2 x ($V_{IL}$(AC) - $V_{REF}$) | NOTE 3 | 2 x ($V_{IL}$(AC) - $V_{REF}$) | V | 2 |

**NOTE:**
1. Used to define a differential signal slew-rate.
2. for CK_t - CK_c use $V_{IHCA}$/$V_{ILCA}$(AC) of ADD/CMD and $V_{REFCA}$;
3. These values are not defined; however, the differential signals CK_t - CK_c, need to be within the respective limits ($V_{IHCA}$(DC) max, $V_{ILCA}$(DC)min) for single-ended signals as well as the limitations for overshoot and undershoot.

**[ Table 9 ] Allowed Time Before Ringback (tDVAC) for CK_t - CK_c**

| Slew Rate [V/ns] | tDVAC [ps] @ $\|V_{IH/Ldiff}(AC)\|$ = 200mV | |
|---|---|---|
| | min | max |
| > 4.0 | 120 | - |
| 4.0 | 115 | - |
| 3.0 | 110 | - |
| 2.0 | 105 | - |
| 1.8 | 100 | - |
| 1.6 | 95 | - |
| 1.4 | 90 | - |
| 1.2 | 85 | - |
| 1.0 | 80 | - |
| < 1.0 | 80 | - |

## 8.3.3 Single-ended Requirements for Differential Signals

Each individual component of a differential signal (CK_t, CK_c) has also to comply with certain requirements for single-ended signals.
CK_t and CK _c have to approximately reach $V_{SEH}$min / $V_{SEL}$max [approximately equal to the ac-levels {$V_{IH.CA}$(AC) / $V_{IL.CA}$(AC)} for ADD/CMD signals] in every half-cycle.
Note that the applicable ac-levels for ADD/CMD might be different per speed-bin etc. E.g. if Different value than $V_{IH.CA}$(AC100)/$V_{IL.CA}$(AC100) is used for ADD/CMD signals, then these ac-levels apply also for the single-ended signals CK_t and CK _c.

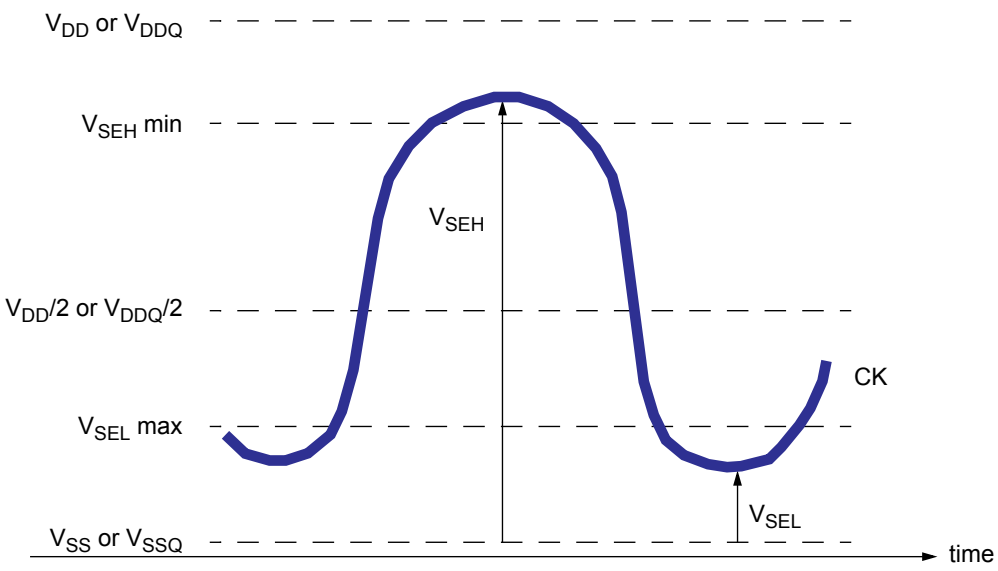



**Figure 3. Single-ended requirement for differential signals**

Note that while ADD/CMD signal requirements are with respect to $V_{REFCA}$, the single-ended components of differential signals have a requirement with respect to $V_{DD}$/2; this is nominally the same. The transition of single-ended signals through the ac-levels is used to measure setup time. For single-ended components of differential signals the requirement to reach $V_{SEL}$max, $V_{SEH}$min has no bearing on timing, but adds a restriction on the common mode characteristics of these signals.

**[ Table 10 ] Single-ended Levels for CK_t, CK_c**

| Symbol | Parameter | DDR4-1600/1866/2133 | | DDR4-2400/2666 | | Unit | NOTE |
|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | | |
| $V_{SEH}$ | Single-ended high-level for CK_t , CK_c | (VDD/2)+0.100 | NOTE3 | TBD | NOTE3 | V | 1, 2 |
| $V_{SEL}$ | Single-ended low-level for CK_t , CK_c | NOTE3 | (VDD/2)-0.100 | NOTE3 | TBD | V | 1, 2 |

NOTE :

1. For CK_t - CK_c use $V_{IH.CA}/V_{IL.CA}$(AC) of ADD/CMD;
2. $V_{IH}$(AC)/$V_{IL}$(AC) for ADD/CMD is based on $V_{REFCA}$;
3. These values are not defined, however the single-ended signals CK_t - CK_c need to be within the respective limits ($V_{IH.CA}$(DC) max, $V_{IL.CA}$(DC)min) for single-ended signals as well as the limitations for overshoot and undershoot.

## 8.3.4 Address, Command and Control Overshoot and Undershoot Specifications

**[ Table 11 ] AC Overshoot/Undershoot Specification for Address, Command and Control Pins**

| Parameter | Symbol | Specification | | | | | Unit | NOTE |
|---|---|---|---|---|---|---|---|---|
| | | DDR4-1600 | DDR4-1866 | DDR4-2133 | DDR4-2400 | DDR4-2666 | | |
| Maximum peak amplitude above VAOS | VAOSP | 0.06 | | | | TBD | V | |
| Upper boundary of overshoot area AAOS1 | VAOS | VDD + 0.24 | | | | TBD | V | 1 |
| Maximum peak amplitude allowed for undershoot | VAUS | 0.30 | | | | TBD | V | |
| Maximum overshoot area per 1 tCK above VAOS | AAOS2 | 0.0083 | 0.0071 | 0.0062 | 0.0055 | TBD | V-ns | |
| Maximum overshoot area per 1 tCK between VDD and VAOS | AAOS1 | 0.2550 | 0.2185 | 0.1914 | 0.1699 | TBD | V-ns | |
| Maximum undershoot area per 1 tCK below VSS | AAUS | 0.2644 | 0.2265 | 0.1984 | 0.1762 | TBD | V-ns | |
| (A0-A13,A17,BG0-BG1,BA0-BA1,ACT_n,RAS_n,CAS_n/A15,WE_n/A14,CS_n,CKE,ODT,C2-C0) | | | | | | | | |

**NOTE:** 1.The value of VAOS matches VDD absolute max as defined in Table 4 Absolute Maximum DC Ratings if VDD equals VDD max as defined in Table 6 Recommended DC Operating Conditions. If VDD is above the recommended operating conditions, VAOS remains at VDD absolute max as defined in Table 4.

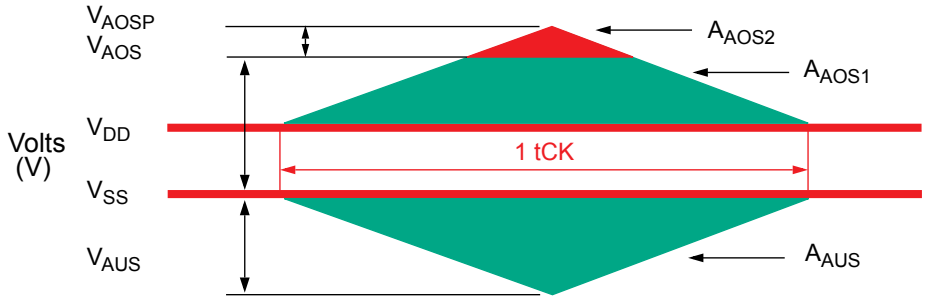



**Figure 4. Address, Command and Control Overshoot and Undershoot Definition**

## 8.3.5 Clock Overshoot and Undershoot Specifications

**[ Table 12 ] AC Overshoot/Undershoot Specification for Clock**

| Parameter | Symbol | Specification | | | | | Unit | NOTE |
|---|---|---|---|---|---|---|---|---|
| | | DDR4-1600 | DDR4-1866 | DDR4-2133 | DDR4-2400 | DDR4-2666 | | |
| Maximum peak amplitude above VCOS | VCOSP | 0.06 | | | | TBD | V | |
| Upper boundary of overshoot area ADOS1 | VCOS | VDD + 0.24 | | | | TBD | V | 1 |
| Maximum peak amplitude allowed for undershoot | VCUS | 0.30 | | | | TBD | V | |
| Maximum overshoot area per 1 UI above VCOS | ACOS2 | 0.0038 | 0.0032 | 0.0028 | 0.0025 | TBD | V-ns | |
| Maximum overshoot area per 1 UI between VDD and VDOS | ACOS1 | 0.1125 | 0.0964 | 0.0844 | 0.0750 | TBD | V-ns | |
| Maximum undershoot area per 1 UI below VSS | ACUS | 0.1144 | 0.0980 | 0.0858 | 0.0762 | TBD | V-ns | |
| (CK_t, CK_c) | | | | | | | | |

**NOTE:** The value of VCOS matches VDD absolute max as defined in Table 4 Absolute Maximum DC Ratings if VDD equals VDD max as defined in Table 6 Recommended DC Operating Conditions. If VDD is above the recommended operating conditions, VCOS remains at VDD absolute max as defined in Table 4.

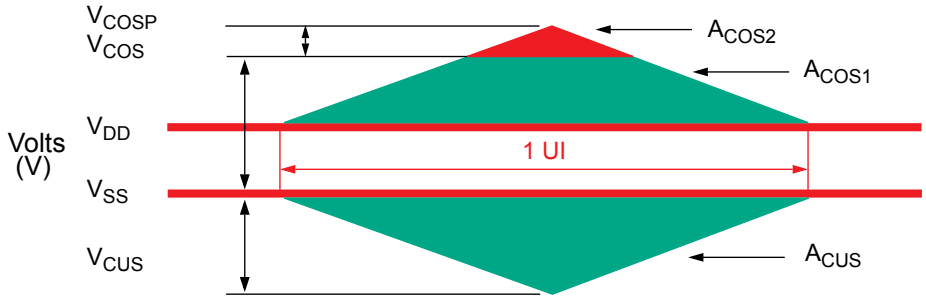



**Figure 5. Clock Overshoot and Undershoot Definition**

## 8.3.6 Data, Strobe and Mask Overshoot and Undershoot Specifications

**[ Table 13 ] AC Overshoot/Undershoot Specification for Data, Strobe and Mask**

| Parameter | Symbol | Specification | | | | | Unit | NOTE |
|---|---|---|---|---|---|---|---|---|
| | | DDR4-1600 | DDR4-1866 | DDR4-2133 | DDR4-2400 | DDR4-2666 | | |
| Maximum peak amplitude above VDOS | VDOSP | 0.16 | 0.16 | 0.16 | 0.16 | TBD | V | |
| Upper boundary of overshoot area ADOS1 | VDOS | VDDQ + 0.24 | | | | TBD | V | 1 |
| Lower boundary of undershoot area ADUS1 | VDUS | 0.30 | 0.30 | 0.30 | 0.30 | TBD | V | 2 |
| Maximum peak amplitude below VDUS | VDUSP | 0.10 | 0.10 | 0.10 | 0.10 | TBD | V | |
| Maximum overshoot area per 1 UI above VDOS | ADOS2 | 0.0150 | 0.0129 | 0.0113 | 0.0100 | TBD | V-ns | |
| Maximum overshoot area per 1 UI between VDDQ and VDOS | ADOS1 | 0.1050 | 0.0900 | 0.0788 | 0.0700 | TBD | V-ns | |
| Maximum undershoot area per 1 UI between VSSQ and VDUS1 | ADUS1 | 0.1050 | 0.0900 | 0.0788 | 0.0700 | TBD | V-ns | |
| Maximum undershoot area per 1 UI below VDUS | ADUS2 | 0.0150 | 0.0129 | 0.0113 | 0.0100 | TBD | V-ns | |
| (DQ, DQS_t, DQS_c, DM_n, DBI_n, TDQS_t, TDQS_c) | | | | | | | | |

**NOTE** :
1. The value of VDOS matches (VIN, VOUT) max as defined in Table 4 Absolute Maximum DC Ratings if VDDQ equals VDDQ max as defined in Table 6 Recommended DC Operating Conditions. If VDDQ is above the recommended operating conditions, VDOS remains at (VIN, VOUT) max as defined in Table 4.
2. The value of VDUS matches (VIN, VOUT) min as defined in Table 4 Absolute Maximum DC Ratings

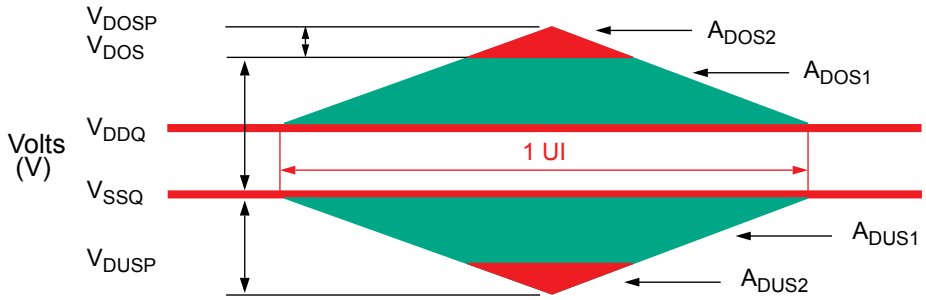



**Figure 6. Data, Strobe and Mask Overshoot and Undershoot Definition**

# 8.4 Slew Rate Definitions

## 8.4.1 Slew Rate Definitions for Differential Input Signals (CK)

Input slew rate for differential signals (CK_t, CK_c) are defined and measured as shown in Table 14 and Figure 7.

**[ Table 14 ] Differential Input Slew Rate Definition**

| Description | Measured | | Defined by |
|---|---|---|---|
| | From | To | |
| Differential input slew rate for rising edge(CK_t - CK_c) | $V_{ILdiffmax}$ | $V_{IHdiffmin}$ | [ $V_{IHdiffmin}$ - $V_{ILdiffmax}$ ] / DeltaTRdiff |
| Differential input slew rate for falling edge(CK_t - CK_c) | $V_{IHdiffmin}$ | $V_{ILdiffmax}$ | [ $V_{IHdiffmin}$ - $V_{ILdiffmax}$ ] / DeltaTFdiff |

**NOTE** :
The differential signal (i.e. CK - $\overline{CK}$ and DQS - $\overline{DQS}$) must be linear between these thresholds.

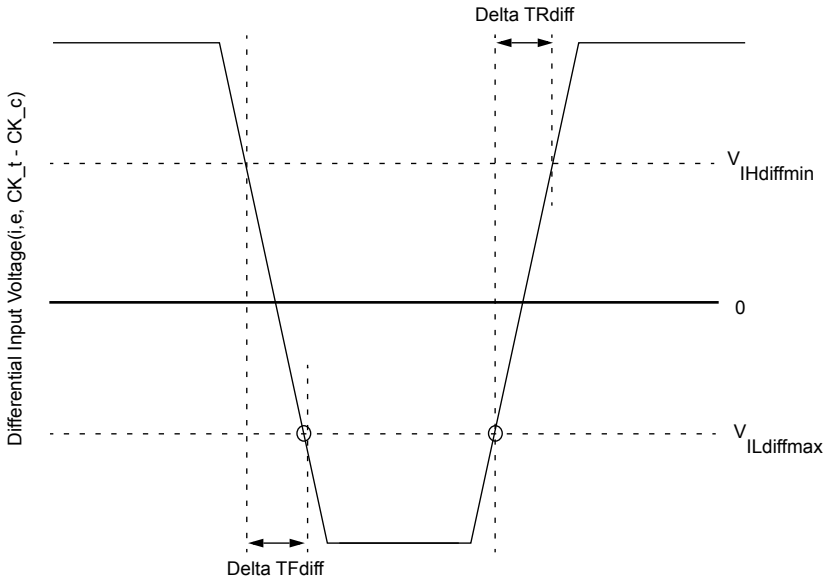
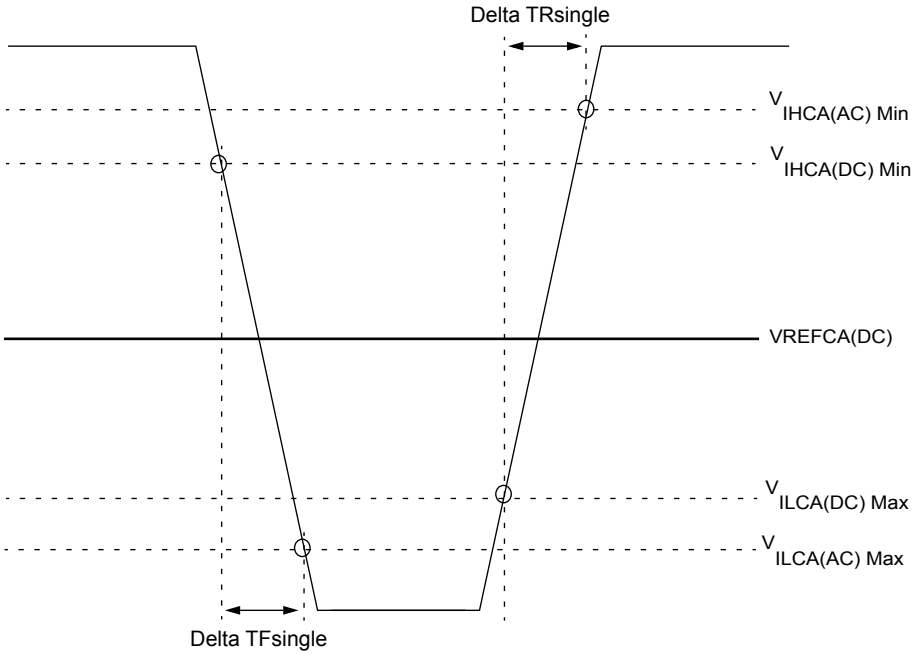



**Figure 7. Differential Input Slew Rate definition for CK, $\overline{CK}$**

## 8.4.2 Slew Rate Definition for Single-ended Input Signals ( CMD/ADD )




**NOTE :**
1. Single-ended input slew rate for rising edge = { VIHCA(AC)Min - VILCA(DC)Max } / Delta TR single
2. Single-ended input slew rate for falling edge = { VIHCA(DC)Min - VILCA(AC)Max } / Delta TF single
3. Single-ended signal rising edge from VILCA(DC)Max to VIHCA(DC)Min must be monotonic slope.
4. Single-ended signal falling edge from VIHCA(DC)Min to VILCA(DC)Max must be monotonic slope.

**Figure 8. Single-ended Input Slew Rate definition for CMD and ADD**

## 8.5 Differential Input Cross Point Voltage

To guarantee tight setup and hold times as well as output skew parameters with respect to clock, each cross point voltage of differential input signals (CK_t, CK_c) must meet the requirements in Table 15. The differential input cross point voltage VIX is measured from the actual cross point of true and complement signals to the midlevel between of VDD and VSS.

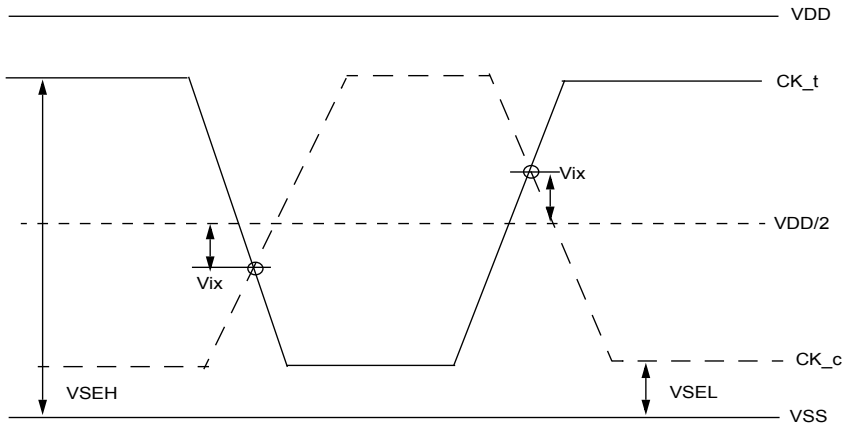



**Figure 9. Vix Definition (CK)**

**[ Table 15 ] Cross Point Voltage for Differential Input Signals (CK)**

| Symbol | Parameter | DDR4-1600/1866/2133 | | | |
|---|---|---|---|---|---|
| | | min | | max | |
| - | Area of VSEH, VSEL | VSEL =< VDD/2 - 145mV | VDD/2 - 145mV =< VSEL =< VDD/2 - 100mV | VDD/2 + 100mV =< VSEH =< VDD/2 + 145mV | VDD/2 + 145mV =< VSEH |
| VIX(CK) | Differential Input Cross Point Voltage relative to VDD/2 for CK_t, CK_c | -120mV | -(VDD/2 - VSEL) + 25mV | (VSEH - VDD/2) - 25mV | 120mV |

| Symbol | Parameter | DDR4-2400/2666 | | | |
|---|---|---|---|---|---|
| | | min | | max | |
| - | Area of VSEH, VSEL | TBD | TBD | TBD | TBD |
| VIX(CK) | Differential Input Cross Point Voltage relative to VDD/2 for CK_t, CK_c | TBD | TBD | TBD | TBD |

# 8.6 CMOS Rail to Rail Input Levels

## 8.6.1 CMOS Rail to Rail Input Levels for RESET_n

**[ Table 16 ] CMOS Rail to Rail Input Levels for RESET_n**

| Parameter | Symbol | Min | Max | Unit | NOTE |
|---|---|---|---|---|---|
| AC Input High Voltage | VIH(AC)_RESET | 0.8*VDD | VDD | V | 6 |
| DC Input High Voltage | VIH(DC)_RESET | 0.7*VDD | VDD | V | 2 |
| DC Input Low Voltage | VIL(DC)_RESET | VSS | 0.3*VDD | V | 1 |
| AC Input Low Voltage | VIL(AC)_RESET | VSS | 0.2*VDD | V | 7 |
| Rising time | TR_RESET | - | 1.0 | us | 4 |
| RESET pulse width | tPW_RESET | 1.0 | - | us | 3,5 |

**NOTE :**

1.After RESET_n is registered LOW, RESET_n level shall be maintained below VIL(DC)_RESET during tPW_RESET, otherwise, SDRAM may not be reset.
2. Once RESET_n is registered HIGH, RESET_n level must be maintained above VIH(DC)_RESET, otherwise, SDRAM operation will not be guaranteed until it is reset asserting RESET_n signal LOW.
3. RESET is destructive to data contents.
4. No slope reversal(ringback) requirement during its level transition from Low to High.
5. This definition is applied only “Reset Procedure at Power Stable”.
6. Overshoot might occur. It should be limited by the Absolute Maximum DC Ratings.
7. Undershoot might occur. It should be limited by Absolute Maximum DC Ratings

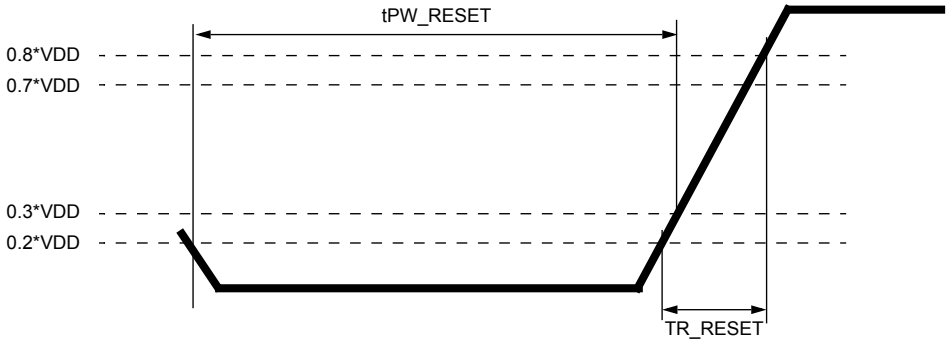



**Figure 10. RESET_n Input Slew Rate Definition**

# 8.7 AC and DC Logic Input Levels for DQS Signals

## 8.7.1 Differential Signal Definition

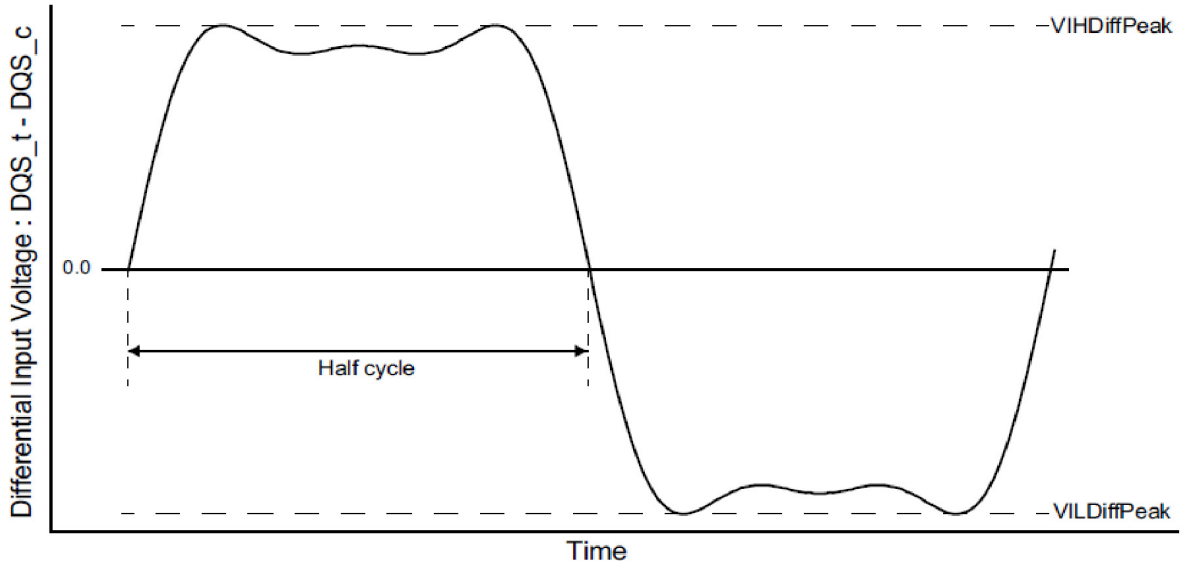



**Figure 11. Definition of differential DQS Signal AC-swing Level**

## 8.7.2 Differential Swing Requirements for DQS (DQS_t - DQS_c)

**[ Table 17 ] Differential AC and DC Input Levels for DQS**

| Symbol | Parameter | DDR4-1600/1866/2133 | | DDR4-2400 | | DDR4-2666 | | Unit | Note |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| VIHDiffPeak | VIH.DIFF.Peak Voltage | 186 | Note2 | 160 | Note2 | TBD | TBD | mV | 1 |
| VILDiffPeak | VIL.DIFF.Peak Voltage | Note2 | -186 | Note2 | -160 | TBD | TBD | mV | 1 |

**NOTE :**

1.Used to define a differential signal slew-rate.

2.These values are not defined; however, the differential signals DQS_t - DQS_c, need to be within the respective limits Overshoot, Undershoot Specification for single-ended signals.

### 8.7.3 Peak Voltage Calculation Method

The peak voltage of Differential DQS signals are calculated in a following equation.

VIH.DIFF.Peak Voltage = Max(f(t))

VIL.DIFF.Peak Voltage = Min(f(t))

f(t) = VDQS_t - VDQS_c

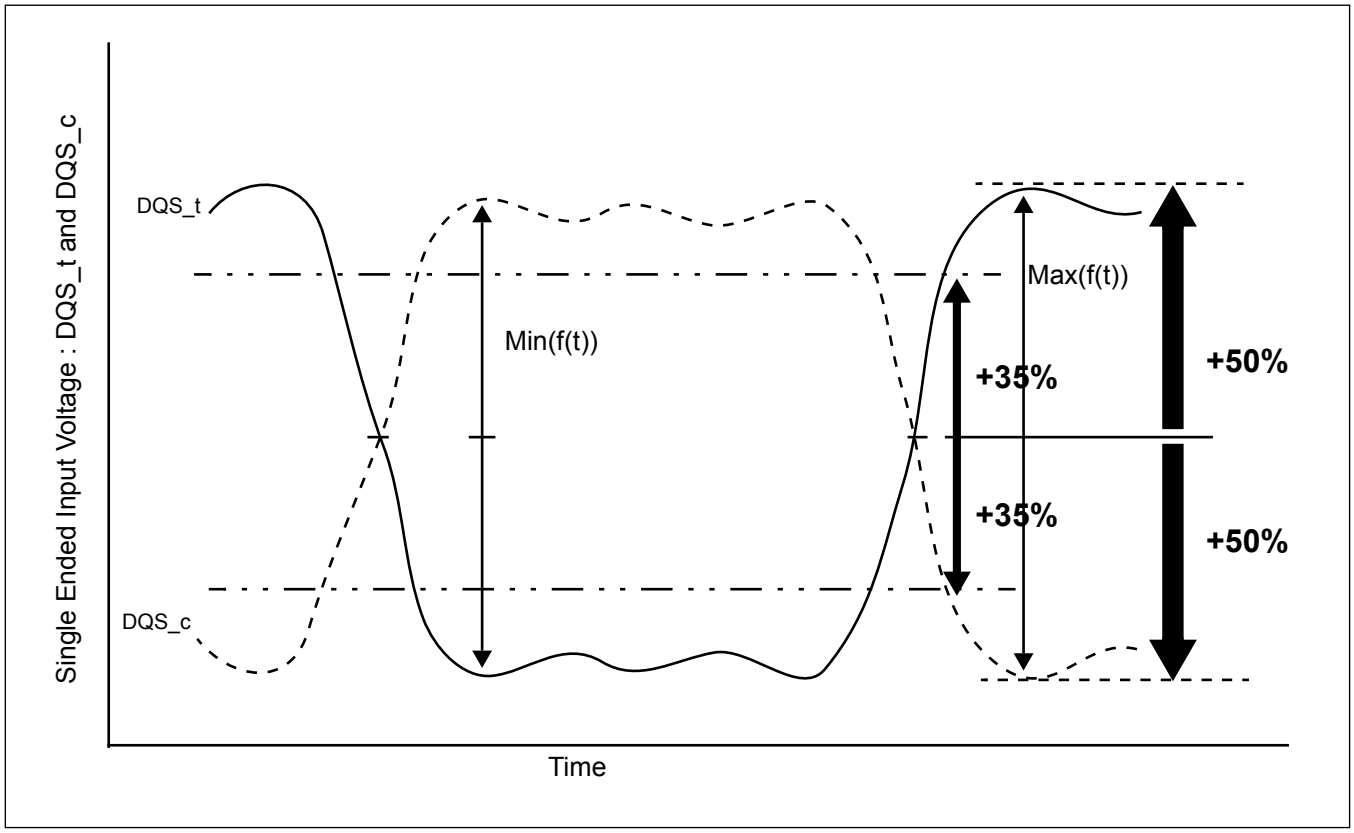



**Figure 12. Definition of differential DQS Peak Voltage and rage of exempt non-monotonic signaling**

## 8.7.4 Differential Input Cross Point Voltage

To achieve tight RxMask input requirements as well as output skew parameters with respect to strobe, the cross point voltage of differential input signals (DQS_t, DQS_c) must meet the requirements in Table 18. The differential input cross point voltage VIX_DQS (VIX_DQS_FR and VIX_DQS_RF) is measured from the actual cross point of DQS_t, DQS_c relative to the VDQSmid of the DQS_t and DQS_c signals.
VDQSmid is the midpoint of the minimum levels achieved by the transitioning DQS_t and DQS_c signals, and noted by VDQS_trans. VDQS_trans is the difference between the lowest horizontal tangent above VDQSmid of the transitioning DQS signals and the highest horizontal tangent below VDQSmid of the transitioning DQS signals.
A non-monotonic transitioning signal's ledge is exempt or not used in determination of a horizontal tangent provided the said ledge occurs within +/- 35% of the midpoint of either VIH.DIFF.Peak Voltage (DQS_t rising) or VIL.DIFF.Peak Voltage (DQS_c rising), refer to Figure 12. A secondary horizontal tangent resulting from a ring-back transition is also exempt in determination of a horizontal tangent. That is, a falling transition's horizontal tangent is derived from its negative slope to zero slope transition (point A in Figure 13) and a ring-back's horizontal tangent derived from its positive slope to zero slope transition (point B in Figure 13) is not a valid horizontal tangent; and a rising transition's horizontal tangent is derived from its positive slope to zero slope transition (point C in Figure 13) and a ring-back's horizontal tangent derived from its negative slope to zero slope transition (point D in Figure 13) is not a valid horizontal tangent

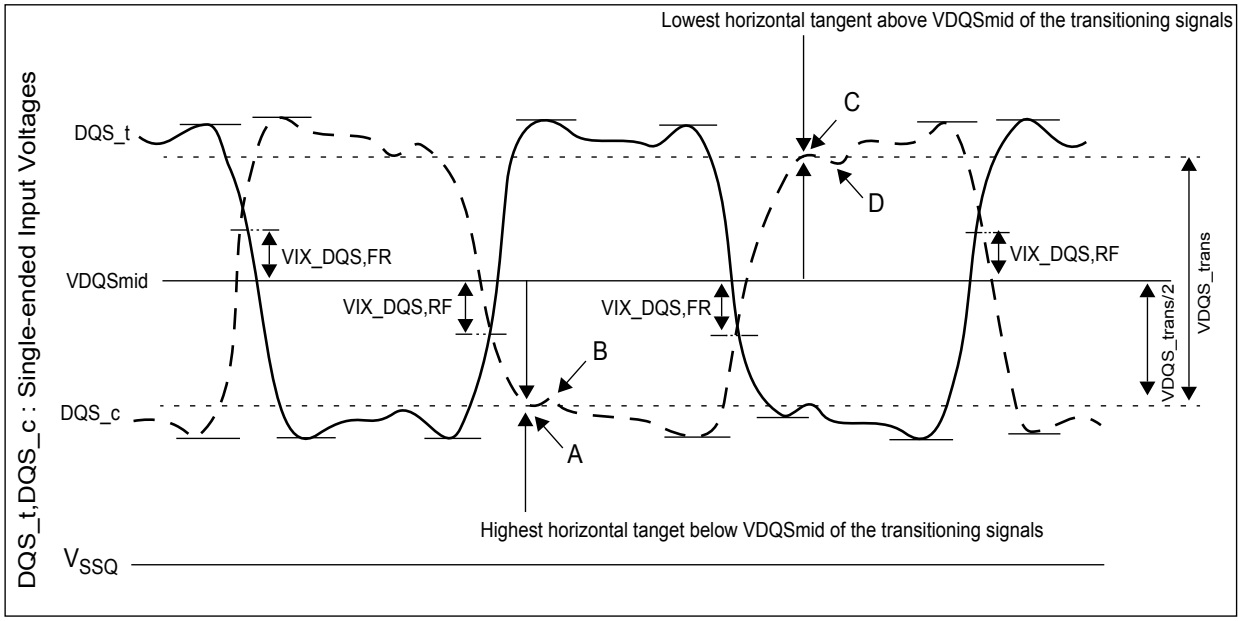



**Figure 13. Vix Definition (DQS)**

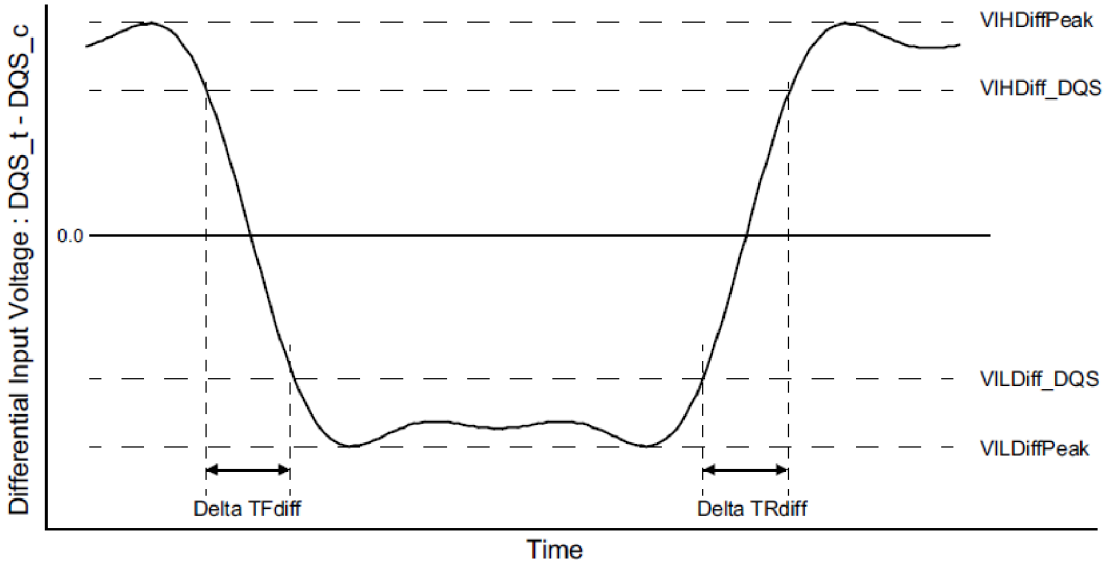
**[ Table 18 ] Cross Point Voltage for DQS Differential Input Signals**

| Symbol | Parameter | DDR4-1600/1866/2133/2400 | | DDR4-2666 | | Unit | Note |
|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | | |
| Vix_DQS_ratio | DQS_t and DQS_c crossing relative to the midpoint of the DQS_t and DQS_c signal swings | - | 25 | - | 25 | % | 1, 2 |
| VDQSmid_to_Vcent | VDQSmid offset relative to Vcent_DQ(midpoint) | - | min(VIHdiff,50) | - | min(VIHdiff,50) | mV | 3, 4, 5 |

**NOTE :**
1. Vix_DQS_Ratio is DQS VIX crossing (Vix_DQS_FR or Vix_DQS_RF) divided by VDQS_trans. VDQS_trans is the difference between the lowest horizontal tangent above VDQSmid of the transitioning DQS signals and the highest horizontal tangent below VDQSmid of the transitioning DQS signals.
2. VDQSmid will be similar to the VREFDQ internal setting value obtained during Vref Training if the DQS and DQs drivers and paths are matched.
3. The maximum limit shall not exceed the smaller of VIHdiff minimum limit or 50mV.
4. VIX measurements are only applicable for transitioning DQS_t and DQS_c signals when toggling data, preamble and high-z states are not applicable conditions.
5. The parameter VDQSmid is defined for simulation and ATE testing purposes, it is not expected to be tested in a system.

## 8.7.5 Differential Input Slew Rate Definition

Input slew rate for differential signals (DQS_t, DQS_c) are defined and measured as shown in are Figure 13 and Figure 14.




**NOTE :**
1. Differential signal rising edge from VILDiff_DQS to VIHDiff_DQS must be monotonic slope.
2. Differential signal falling edge from VIHDiff_DQS to VILDiff_DQS must be monotonic slope.

**Figure 14. Differential Input Slew Rate Definition for DQS_t, DQS_c**

**[ Table 19 ] Differential Input Slew Rate Definition for DQS_t, DQS_c**

| Description | From | To | Defined by |
|---|---|---|---|
| Differential input slew rate for rising edge(DQS_t - DQS_c) | VILDiff_DQS | VIHDiff_DQS | \|VILDiff_DQS - VIHDiff_DQS\|/DeltaTRdiff |
| Differential input slew rate for falling edge(DQS_t - DQS_c) | VIHDiff_DQS | VILDiff_DQS | \|VILDiff_DQS - VIHDiff_DQS\|/DeltaTFdiff |

**[ Table 20 ] Differential Input Level for DQS_t, DQS_c**

| Symbol | Parameter | DDR4-1600/1866/2133 | | DDR4-2400 | | DDR4-2666 | | Unit | NOTE |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| VIHDiff_DQS | Differntial Input High | 136 | - | 130 | - | TBD | TBD | mV | |
| VILDiff_DQS | Differntial Input Low | - | -136 | - | -130 | TBD | TBD | mV | |

**[ Table 21 ] Differential Input Slew Rate for DQS_t, DQS_c**

| Symbol | Parameter | DDR4-1600/1866/2133/2400 | | DDR4-2666 | | Unit | NOTE |
|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | | |
| SRIdiff | Differential Intput Slew Rate | 3 | 18 | TBD | TBD | V/ns | |

# 9. AC and DC Output Measurement Levels

## 9.1 Output Driver DC Electrical Characteristics

The DDR4 driver supports two different Ron values. These Ron values are referred as strong(low Ron) and weak mode(high Ron). A functional representation of the output buffer is shown in the figure below. Output driver impedance RON is defined as follows:

The individual pull-up and pull-down resistors ($RON_{Pu}$ and $RON_{Pd}$) are defined as follows:

$$RON_{Pu} = \frac{VDDQ - Vout}{|I\ out|}$$ under the condition that $RON_{Pd}$ is off

$$RON_{Pd} = \frac{Vout}{|I\ out|}$$ under the condition that $RON_{Pu}$ is off

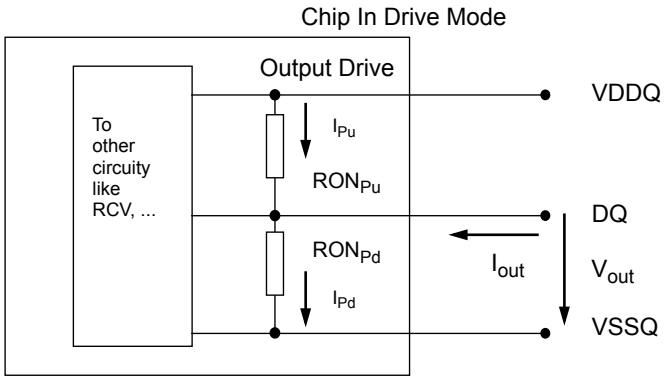



**Figure 15. Output driver**

**[ Table 22 ] Output Driver DC Electrical Characteristics, assuming RZQ=240ohm; entire operating temperature range; after proper ZQ calibration**

| $RON_{NOM}$ | Resistor | Vout | Min | Nom | Max | Unit | NOTE |
|---|---|---|---|---|---|---|---|
| 34Ω | RON34Pd | VOLdc= 0.5*VDDQ | 0.8 | 1 | 1.1 | RZQ/7 | 1,2 |
| | | VOMdc= 0.8* VDDQ | 0.9 | 1 | 1.1 | RZQ/7 | 1,2 |
| | | VOHdc= 1.1* VDDQ | 0.9 | 1 | 1.25 | RZQ/7 | 1,2 |
| | RON34Pu | VOLdc= 0.5* VDDQ | 0.9 | 1 | 1.25 | RZQ/7 | 1,2 |
| | | VOMdc= 0.8* VDDQ | 0.9 | 1 | 1.1 | RZQ/7 | 1,2 |
| | | VOHdc= 1.1* VDDQ | 0.8 | 1 | 1.1 | RZQ/7 | 1,2 |
| 48Ω | RON48Pd | VOLdc= 0.5*VDDQ | 0.8 | 1 | 1.1 | RZQ/5 | 1,2 |
| | | VOMdc= 0.8* VDDQ | 0.9 | 1 | 1.1 | RZQ/5 | 1,2 |
| | | VOHdc= 1.1* VDDQ | 0.9 | 1 | 1.25 | RZQ/5 | 1,2 |
| | RON48Pu | VOLdc= 0.5* VDDQ | 0.9 | 1 | 1.25 | RZQ/5 | 1,2 |
| | | VOMdc= 0.8* VDDQ | 0.9 | 1 | 1.1 | RZQ/5 | 1,2 |
| | | VOHdc= 1.1* VDDQ | 0.8 | 1 | 1.1 | RZQ/5 | 1,2 |
| Mismatch between pull-up and pull-down, MMPuPd | | VOMdc= 0.8* VDDQ | -10 | - | 10 | % | 1,2,3,4 |
| Mismatch DQ-DQ within byte variation pull-up, MMPudd | | VOMdc= 0.8* VDDQ | - | - | 10 | % | 1,2,4 |
| Mismatch DQ-DQ within byte variation pull-dn, MMPddd | | VOMdc= 0.8* VDDQ | - | - | 10 | % | 1,2,4 |

**NOTE :**

1. The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see following section on voltage and temperature sensitivity(TBD).
2. Pull-up and pull-dn output driver impedances are recommended to be calibrated at 0.8 * VDDQ. Other calibration schemes may be used to achieve the linearity spec shown above, e.g. calibration at 0.5 * VDDQ and 1.1 * VDDQ.
3. Measurement definition for mismatch between pull-up and pull-down, MMPuPd : Measure RONPu and RONPD both at 0.8*VDD separately; Ronnom is the nominal Ron value

$$MMPuPd = \frac{RONPu - RONPd}{RONNOM} * 100$$

4. RON variance range ratio to RON Nominal value in a given component, including DQS_t and DQS_c.

$$MMPudd = \frac{RONPuMax - RONPuMin}{RONNOM} * 100$$

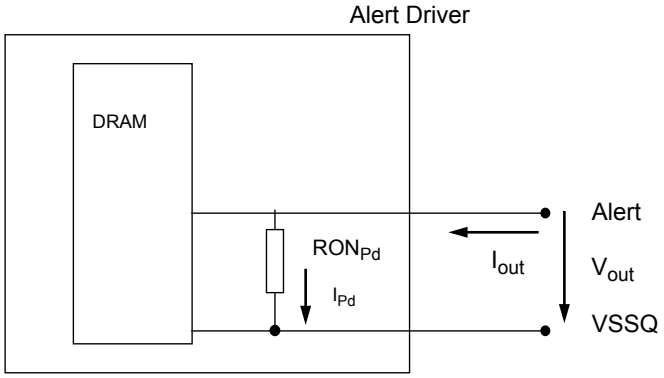
$$MMPddd = \frac{RONPdMax - RONPdMin}{RONNOM} * 100$$

5. This parameter of x16 device is specified for Upper byte and Lower byte.

## 9.1.1 Alert_n Output Drive Characteristic

A functional representation of the output buffer is shown in the figure below. Output driver impedance RON is defined as follows:

$$RON_{Pd} = \frac{Vout}{|\ Iout\ |}$$ under the condition that $RON_{Pu}$ is off




| Resistor | Vout | Min | Max | Unit | NOTE |
|---|---|---|---|---|---|
| $RON_{Pd}$ | VOLdc= 0.1* VDDQ | 0.3 | 1.2 | 34Ω | 1 |
| | $V_{OMdc}$ = 0.8* VDDQ | 0.4 | 1.2 | 34Ω | 1 |
| | $V_{OHdc}$ = 1.1* VDDQ | 0.4 | 1.4 | 34Ω | 1 |

**NOTE :**
1. VDDQ voltage is at VDDQ DC. VDDQ DC definition is TBD.

## 9.1.2 Output Driver Characteristic of Connectivity Test ( CT ) Mode

Following Output driver impedance RON will be applied Test Output Pin during Connectivity Test ( CT ) Mode.
The individual pull-up and pull-down resistors (RONPu_CT and RONPd_CT) are defined as follows:

$$RON_{Pu_CT} = \frac{V_{DDQ}-V_{OUT}}{|\ Iout\ |}$$

$$RON_{Pd_CT} = \frac{V_{OUT}}{|\ Iout\ |}$$

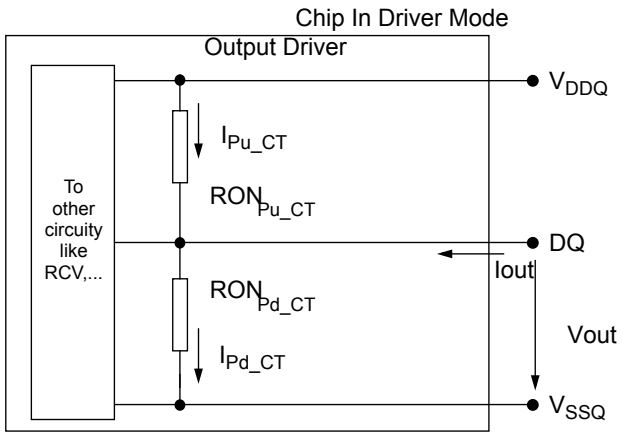



**Figure 16. Output Driver**

| $RON_{NOM_CT}$ | Resistor | Vout | Max | Units | NOTE |
|---|---|---|---|---|---|
| 34Ω | $RON_{Pd_CT}$ | $VOB_{dc}$ = 0.2 x $V_{DDQ}$ | 1.9 | 34Ω | 1 |
| | | $VOL_{dc}$ = 0.5 x $V_{DDQ}$ | 2.0 | 34Ω | 1 |
| | | $VOM_{dc}$ = 0.8 x $V_{DDQ}$ | 2.2 | 34Ω | 1 |
| | | $VOH_{dc}$ = 1.1 x $V_{DDQ}$ | 2.5 | 34Ω | 1 |
| | $RON_{Pu_CT}$ | $VOB_{dc}$ = 0.2 x $V_{DDQ}$ | 2.5 | 34Ω | 1 |
| | | $VOL_{dc}$ = 0.5 x $V_{DDQ}$ | 2.2 | 34Ω | 1 |
| | | $VOM_{dc}$ = 0.8 x $V_{DDQ}$ | 2.0 | 34Ω | 1 |
| | | $VOH_{dc}$ = 1.1 x $V_{DDQ}$ | 1.9 | 34Ω | 1 |

**NOTE :**
1. Connectivity test mode uses un-calibrated drivers, showing the full range over PVT. No mismatch between pull up and pull down is defined.

## 9.2 Single-ended AC & DC Output Levels

**[ Table 23 ] Single-ended AC & DC Output Levels**

| Symbol | Parameter | DDR4-1600/1866/2133/2400/2666 | Units | NOTE |
|---|---|---|---|---|
| $V_{OH}$(DC) | DC output high measurement level (for IV curve linearity) | 1.1 x $V_{DDQ}$ | V | |
| $V_{OM}$(DC) | DC output mid measurement level (for IV curve linearity) | 0.8 x $V_{DDQ}$ | V | |
| $V_{OL}$(DC) | DC output low measurement level (for IV curve linearity) | 0.5 x $V_{DDQ}$ | V | |
| $V_{OH}$(AC) | AC output high measurement level (for output SR) | (0.7 + 0.15) x $V_{DDQ}$ | V | 1 |
| $V_{OL}$(AC) | AC output low measurement level (for output SR) | (0.7 - 0.15) x $V_{DDQ}$ | V | 1 |

**NOTE** :
1. The swing of ± 0.15 × $V_{DDQ}$ is based on approximately 50% of the static single-ended output peak-to-peak swing with a driver impedance of RZQ/7Ω and an effective test load of 50Ω to $V_{TT}$ = $V_{DDQ}$.

## 9.3 Differential AC & DC Output Levels

**[ Table 24 ] Differential AC & DC Output Levels**

| Symbol | Parameter | DDR4-1600/1866/2133/2400/2666 | Units | NOTE |
|---|---|---|---|---|
| $V_{OHdiff}$(AC) | AC differential output high measurement level (for output SR) | +0.3 x $V_{DDQ}$ | V | 1 |
| $V_{OLdiff}$(AC) | AC differential output low measurement level (for output SR) | -0.3 x $V_{DDQ}$ | V | 1 |

**NOTE** :
1. The swing of ± 0.3 × $V_{DDQ}$ is based on approximately 50% of the static differential output peak-to-peak swing with a driver impedance of RZQ/7Ω and an effective test load of 50Ω to $V_{TT}$ = $V_{DDQ}$ at each of the differential outputs.

## 9.4 Single-ended Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between $V_{OL(AC)}$ and $V_{OH(AC)}$ for single ended signals as shown in Table 25 and Figure 17.

**[ Table 25 ] Single-ended Output Slew Rate Definition**

| Description | Measured | | Defined by |
|---|---|---|---|
| | From | To | |
| Single ended output slew rate for rising edge | $V_{OL}$(AC) | $V_{OH}$(AC) | [$V_{OH}$(AC)-$V_{OL}$(AC)] / Delta TRse |
| Single ended output slew rate for falling edge | $V_{OH}$(AC) | $V_{OL}$(AC) | [$V_{OH}$(AC)-$V_{OL}$(AC)] / Delta TFse |

**NOTE** :
1. Output slew rate is verified by design and characterization, and may not be subject to production test.

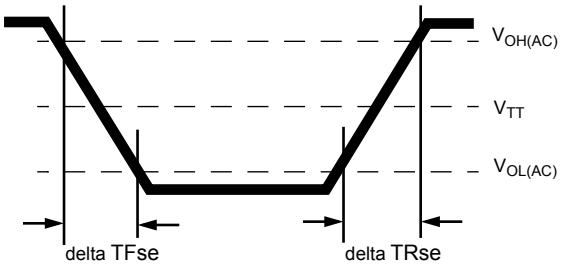



**Figure 17. Single-ended Output Slew Rate Definition**

**[ Table 26 ] Single-ended Output Slew Rate**

| Parameter | Symbol | DDR4-1600 | | DDR4-1866 | | DDR4-2133 | | DDR4-2400 | | DDR4-2666 | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | |
| Single ended output slew rate | SRQse | 4 | 9 | 4 | 9 | 4 | 9 | 4 | 9 | 4 | 9 | V/ns |

Description: SR: Slew Rate
Q: Query Output (like in DQ, which stands for Data-in, Query-Output)
se: Single-ended Signals
For Ron = RZQ/7 setting

**NOTE :**
1. In two cases, a maximum slew rate of 12 V/ns applies for a single DQ signal within a byte lane.
-Case 1 is defined for a single DQ signal within a byte lane which is switching into a certain direction (either from high to low or low to high) while all remaining DQ signals in the same byte lane are static (i.e. they stay at either high or low).
-Case 2 is defined for a single DQ signal within a byte lane which is switching into a certain direction (either from high to low or low to high) while all remaining DQ signals in the same byte lane are switching into the opposite direction (i.e. from low to high or high to low respectively). For the remaining DQ signal switching into the opposite direction, the regular maximum limit of 9 V/ns applies

## 9.5 Differential Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between VOLdiff(AC) and VOHdiff(AC) for differential signals as shown in Table 27 and Figure 18.

**[ Table 27 ] Differential Output Slew Rate Definition**

| Description | Measured | | Defined by |
|---|---|---|---|
| | From | To | |
| Differential output slew rate for rising edge | $V_{OLdiff}(AC)$ | $V_{OHdiff}(AC)$ | $[V_{OHdiff}(AC)-V_{OLdiff}(AC)]$ / Delta TRdiff |
| Differential output slew rate for falling edge | $V_{OHdiff}(AC)$ | $V_{OLdiff}(AC)$ | $[V_{OHdiff}(AC)-V_{OLdiff}(AC)]$ /Delta TFdiff |

**NOTE** :
1. Output slew rate is verified by design and characterization, and may not be subject to production test.

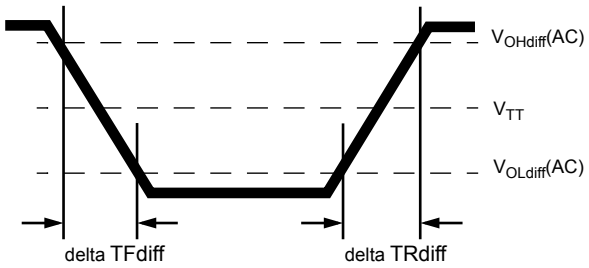



**Figure 18. Differential Output Slew Rate Definition**

**[ Table 28 ] Differential Output Slew Rate**

| Parameter | Symbol | DDR4-1600 | | DDR4-1866 | | DDR4-2133 | | DDR4-2400 | | DDR4-2666 | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | |
| Differential output slew rate | SRQdiff | 8 | 18 | 8 | 18 | 8 | 18 | 8 | 18 | 8 | 18 | V/ns |

Description:
SR: Slew Rate
Q: Query Output (like in DQ, which stands for Data-in, Query-Output)
diff: Differential Signals
For Ron = RZQ/7 setting

## 9.6 Single-ended AC & DC Output Levels of Connectivity Test Mode

Following output parameters will be applied for DDR4 SDRAM Output Signal during Connectivity Test Mode.

**[ Table 29 ] Single-ended AC & DC Output Levels of Connectivity Test Mode**

| Symbol | Parameter | DDR4-1600/1866/2133 /2400/2666 | Unit | Notes |
|---|---|---|---|---|
| $V_{OH(DC)}$ | DC output high measurement level (for IV curve linearity) | 1.1 x VDDQ | V | |
| $V_{OM(DC)}$ | DC output mid measurement level (for IV curve linearity) | 0.8 x VDDQ | V | |
| $V_{OL(DC)}$ | DC output low measurement level (for IV curve linearity) | 0.5 x VDDQ | V | |
| $V_{OB(DC)}$ | DC output below measurement level (for IV curve linearity) | 0.2 x VDDQ | V | |
| $V_{OH(AC)}$ | AC output high measurement level (for output SR) | VTT + (0.1 x VDDQ) | V | 1 |
| $V_{OL(AC)}$ | AC output below measurement level (for output SR) | VTT - (0.1 x VDDQ) | V | 1 |

**NOTE**

1. The effective test load is 50Ω terminated by VTT = 0.5 * VDDQ.

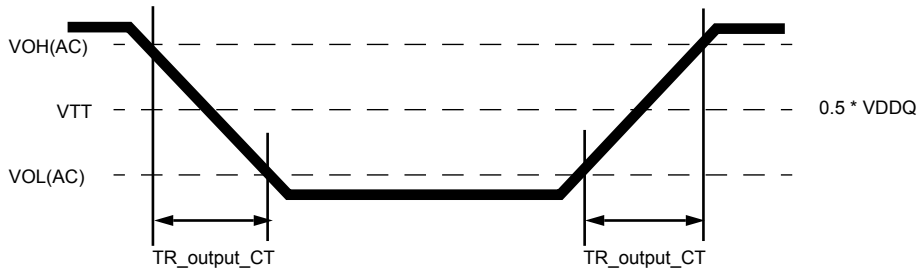



**Figure 19. Output Slew Rate Definition of Connectivity Test Mode**

**[ Table 30 ] Single-ended Output Slew Rate of Connectivity Test Mode**

| Parameter | Symbol | DDR4-1600/1866/2133/2400/2666 | | Unit | Notes |
|---|---|---|---|---|---|
| | | Min | Max | | |
| Output signal Falling time | TF_output_CT | - | 10 | ns/V | |
| Output signal Rising time | TR_output_CT | - | 10 | ns/V | |

## 9.7 Test Load for Connectivity Test Mode Timing

The reference load for ODT timings is defined in Figure 20.

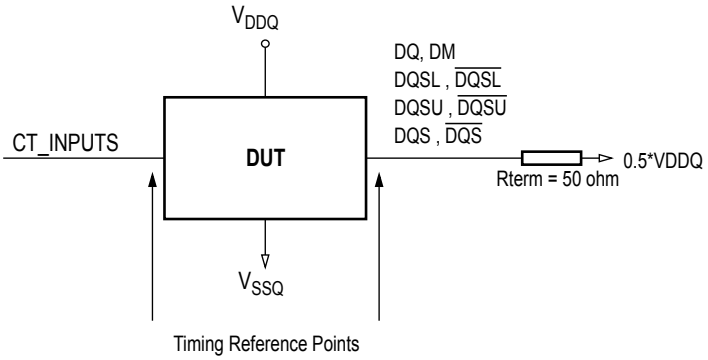



**Figure 20. Connectivity Test Mode Timing Reference Load**

# 10. Speed Bin

**[ Table 31 ] DDR4-1600 Speed Bins and Operations**

| Speed Bin | | | | DDR4-1600 | | Unit | NOTE |
|---|---|---|---|---|---|---|---|
| CL-nRCD-nRP | | | | 11-11-11 | | | |
| Parameter | | | Symbol | min | max | | |
| Internal read command to first data | | | tAA | 13.75[13]<br>(13.50)[5,11] | 18.00 | ns | 11 |
| Internal read command to first data with read DBI enabled | | | tAA_DBI | tAA(min) + 2nCK | tAA(max) +2nCK | ns | 11 |
| ACT to internal read or write delay time | | | tRCD | 13.75<br>(13.50)[5,11] | - | ns | 11 |
| PRE command period | | | tRP | 13.75<br>(13.50)[5,11] | - | ns | 11 |
| ACT to PRE command period | | | tRAS | 35 | 9 x tREFI | ns | 11 |
| ACT to ACT or REF command period | | | tRC | 48.75<br>(48.50)[5,11] | - | ns | 11 |
| | Normal | Read DBI | | | | | |
| CWL = 9 | CL = 9 | CL = 11 | tCK(AVG) | 1.5<br>(Optional)[5,11] | 1.6 | ns | 1,2,3,4,10,13 |
| | CL = 10 | CL = 12 | tCK(AVG) | Reserved | | ns | 1,2,3,4,10 |
| CWL = 9,11 | CL = 10 | CL = 12 | tCK(AVG) | Reserved | | ns | 1,2,3,4 |
| | CL = 11 | CL = 13 | tCK(AVG) | 1.25 | <1.5 | ns | 1,2,3,4 |
| | CL = 12 | CL = 14 | tCK(AVG) | 1.25 | <1.5 | ns | 1,2,3 |
| Supported CL Settings | | | | 9,11,12 | | nCK | 12,13 |
| Supported CL Settings with read DBI | | | | 11,13,14 | | nCK | 12 |
| Supported CWL Settings | | | | 9,11 | | nCK | |

**[ Table 32 ] DDR4-1866 Speed Bins and Operations**

| Speed Bin | | | | DDR4-1866 | | Unit | NOTE |
|---|---|---|---|---|---|---|---|
| CL-nRCD-nRP | | | | 13-13-13 | | | |
| Parameter | | | Symbol | min | max | | |
| Internal read command to first data | | | tAA | 13.92[13]<br>(13.50)[5,11] | 18.00 | ns | 11 |
| Internal read command to first data with read DBI enabled | | | tAA_DBI | tAA(min) + 2nCK | tAA(max) +2nCK | ns | 11 |
| ACT to internal read or write delay time | | | tRCD | 13.92<br>(13.50)[5,11] | - | ns | 11 |
| PRE command period | | | tRP | 13.92<br>(13.50)[5,11] | - | ns | 11 |
| ACT to PRE command period | | | tRAS | 34 | 9 x tREFI | ns | 11 |
| ACT to ACT or REF command period | | | tRC | 47.92<br>(47.50)[5,11] | - | ns | 11 |
| | Normal | Read DBI | | | | | |
| CWL = 9 | CL = 9 | CL = 11 | tCK(AVG) | 1.5<br>(Optional)[5,11] | 1.6 | ns | 1,2,3,4,10,13 |
| | CL = 10 | CL = 12 | tCK(AVG) | Reserved | | ns | 1,2,3,4,10 |
| CWL = 9,11 | CL = 10 | CL = 12 | tCK(AVG) | Reserved | | ns | 4 |
| | CL = 11 | CL = 13 | tCK(AVG) | 1.25<br>(Optional)[5,11] | <1.5 | ns | 1,2,3,4,6 |
| | CL = 12 | CL = 14 | tCK(AVG) | 1.25 | <1.5 | ns | 1,2,3,6 |
| CWL = 10,12 | CL = 12 | CL = 14 | tCK(AVG) | Reserved | | ns | 1,2,3,4 |
| | CL = 13 | CL = 15 | tCK(AVG) | 1.071 | <1.25 | ns | 1,2,3,4 |
| | CL = 14 | CL = 16 | tCK(AVG) | 1.071 | <1.25 | ns | 1,2,3 |
| Supported CL Settings | | | | 9,11,12,13,14 | | nCK | 12,13 |
| Supported CL Settings with read DBI | | | | 11,13,14,15,16 | | nCK | 12 |
| Supported CWL Settings | | | | 9,10,11,12 | | nCK | |

**[ Table 33 ] DDR4-2133 Speed Bins and Operations**

| Speed Bin | | | | DDR4-2133 | | Unit | NOTE |
|---|---|---|---|---|---|---|---|
| CL-nRCD-nRP | | | | 15-15-15 | | | |
| Parameter | | | Symbol | min | max | | |
| Internal read command to first data | | | tAA | 14.06[13]<br>(13.75)[5,11] | 18.00 | ns | 11 |
| Internal read command to first data with read DBI enabled | | | tAA_DBI | tAA(min) + 3nCK | tAA(max) + 3nCK | ns | 11 |
| ACT to internal read or write delay time | | | tRCD | 14.06<br>(13.75)[5,11] | - | ns | 11 |
| PRE command period | | | tRP | 14.06<br>(13.75)[5,11] | - | ns | 11 |
| ACT to PRE command period | | | tRAS | 33 | 9 x tREFI | ns | 11 |
| ACT to ACT or REF command period | | | tRC | 47.06<br>(46.75)[5,11] | - | ns | 11 |
| | Normal | Read DBI | | | | | |
| CWL = 9 | CL = 9 | CL = 11 | tCK(AVG) | 1.5<br>(Optional)[5,11] | 1.6 | ns | 1,2,3,4,10,13 |
| | CL = 10 | CL = 12 | tCK(AVG) | Reserved | | ns | 1,2,3,10 |
| CWL = 9,11 | CL = 11 | CL = 13 | tCK(AVG) | 1.25<br>(Optional)[5,11] | <1.5 | ns | 1,2,3,4,7 |
| | CL = 12 | CL = 14 | tCK(AVG) | 1.25 | <1.5 | ns | 1,2,3,7 |
| CWL = 10,12 | CL = 13 | CL = 15 | tCK(AVG) | 1.071<br>(Optional)[5,11] | <1.25 | ns | 1,2,3,4,7 |
| | CL = 14 | CL = 16 | tCK(AVG) | 1.071 | <1.25 | ns | 1,2,3,7 |
| CWL = 11,14 | CL = 14 | CL = 17 | tCK(AVG) | Reserved | | ns | 1,2,3,4 |
| | CL = 15 | CL = 18 | tCK(AVG) | 0.937 | <1.071 | ns | 1,2,3,4 |
| | CL = 16 | CL = 19 | tCK(AVG) | 0.937 | <1.071 | ns | 1,2,3 |
| Supported CL Settings | | | | 9,11.12,13,14,15,16 | | nCK | 12,13 |
| Supported CL Settings with read DBI | | | | 11,13,14,15,16,18,19 | | nCK | |
| Supported CWL Settings | | | | 9,10,11,12,14 | | nCK | |

**[ Table 34 ] DDR4-2400 Speed Bins and Operations**

| Speed Bin | | | | DDR4-2400 | | Unit | NOTE |
|---|---|---|---|---|---|---|---|
| CL-nRCD-nRP | | | | 17-17-17 | | | |
| Parameter | | | Symbol | min | max | | |
| Internal read command to first data | | | tAA | 14.16<br>(13.75)[5,11] | 18.00 | ns | 11 |
| Internal read command to first data with read DBI enabled | | | tAA_DBI | tAA(min) + 3nCK | tAA(max) + 3nCK | ns | 11 |
| ACT to internal read or write delay time | | | tRCD | 14.16<br>(13.75)[5,11] | - | ns | 11 |
| PRE command period | | | tRP | 14.16<br>(13.75)[5,11] | - | ns | 11 |
| ACT to PRE command period | | | tRAS | 32 | 9 x tREFI | ns | 11 |
| ACT to ACT or REF command period | | | tRC | 46.16<br>(45.75)[5,11] | - | ns | 11 |
| | Normal | Read DBI | | | | | |
| CWL = 9 | CL = 9 | CL = 11 | tCK(AVG) | Reserved | | ns | 1,2,3,4,9 |
| | CL = 10 | CL = 12 | tCK(AVG) | 1.5 | 1.6 | ns | 1,2,3,4,9 |
| CWL = 9,11 | CL = 10 | CL = 12 | tCK(AVG) | Reserved | | ns | 4 |
| | CL = 11 | CL = 13 | tCK(AVG) | 1.25 | <1.5 | ns | 1,2,3,4,8 |
| | | | | (Optional)[5,11] | | | |
| | CL = 12 | CL = 14 | tCK(AVG) | 1.25 | <1.5 | ns | 1,2,3,8 |
| CWL = 10,12 | CL = 12 | CL = 14 | tCK(AVG) | Reserved | | ns | 4 |
| | CL = 13 | CL = 15 | tCK(AVG) | 1.071 | <1.25 | ns | 1,2,3,4,8 |
| | | | | (Optional)[5,11] | | | |
| | CL = 14 | CL = 16 | tCK(AVG) | 1.071 | <1.25 | ns | 1,2,3,8 |
| CWL = 11,14 | CL = 14 | CL = 17 | tCK(AVG) | Reserved | | ns | 4 |
| | CL = 15 | CL = 18 | tCK(AVG) | 0.937 | <1.071 | ns | 1,2,3,4,8 |
| | | | | (Optional)[5,11] | | | |
| | CL = 16 | CL = 19 | tCK(AVG) | 0.937 | <1.071 | ns | 1,2,3,8 |
| CWL = 12,16 | CL = 15 | CL = 18 | tCK(AVG) | Reserved | | ns | 1,2,3,4 |
| | CL = 16 | CL = 19 | tCK(AVG) | Reserved | | ns | 1,2,3,4 |
| | CL = 17 | CL = 20 | tCK(AVG) | 0.833 | <0.937 | | |
| | CL = 18 | CL = 21 | tCK(AVG) | 0.833 | <0.937 | ns | 1,2,3 |
| Supported CL Settings | | | | 10,11,12,13,14,15,16,17,18 | | nCK | 12,13 |
| Supported CL Settings with read DBI | | | | 12,13,14,15,16,18,19,20,21 | | nCK | |
| Supported CWL Settings | | | | 9,10,11,12,14,16 | | nCK | |

**[ Table 35 ] DDR4-2666 Speed Bins and Operations**

| Speed Bin | | | | DDR4-2666 | | Unit | NOTE |
|---|---|---|---|---|---|---|---|
| CL-nRCD-nRP | | | | 19-19-19 | | | |
| Parameter | | | Symbol | min | max | | |
| Internal read command to first data | | | tAA | 14.25[14] (13.75)[5,12] | 18.00 | ns | 11 |
| Internal read command to first data with read DBI enabled | | | tAA_DBI | tAA(min) + 3nCK | tAA(max) + 3nCK | ns | 11 |
| ACT to internal read or write delay time | | | tRCD | 14.25 (13.75)[5,12] | - | ns | 11 |
| PRE command period | | | tRP | 14.25[14] (13.75)[5,12] | - | ns | 11 |
| ACT to PRE command period | | | tRAS | 32 | 9 x tREFI | ns | 11 |
| ACT to ACT or REF command period | | | tRC | 46.25 (45.75)[5,12] | - | ns | 11 |
| | Normal | Read DBI | | | | | |
| CWL = 9 | CL = 9 | CL = 11 | tCK(AVG) | Reserved | | ns | 1,2,3,4,10 |
| | CL = 10 | CL = 12 | tCK(AVG) | 1.5 | 1.6 | ns | 1,2,3,10 |
| CWL = 9,11 | CL = 10 | CL = 12 | tCK(AVG) | Reserved | | ns | 4 |
| | CL = 11 | CL = 13 | tCK(AVG) | 1.25 | <1.5 | ns | 1,2,3,4,9 |
| | | | | (Optional)[5,12] | | | |
| | CL = 12 | CL = 14 | tCK(AVG) | 1.25 | <1.5 | ns | 1,2,3,9 |
| CWL = 10,12 | CL = 12 | CL = 14 | tCK(AVG) | Reserved | | ns | 4 |
| | CL = 13 | CL = 15 | tCK(AVG) | 1.071 | <1.25 | ns | 1,2,3,4,9 |
| | | | | (Optional)[5,12] | | | |
| | CL = 14 | CL = 16 | tCK(AVG) | 1.071 | <1.25 | ns | 1,2,3,9 |
| CWL = 11,14 | CL = 14 | CL = 17 | tCK(AVG) | Reserved | | ns | 4 |
| | CL = 15 | CL = 18 | tCK(AVG) | 0.937 | <1.071 | ns | 1,2,3,4,9 |
| | | | | (Optional)[5,12] | | | |
| | CL = 16 | CL = 19 | tCK(AVG) | 0.937 | <1.071 | ns | 1,2,3,9 |
| CWL = 12,16 | CL = 15 | CL = 18 | tCK(AVG) | Reserved | | ns | 4 |
| | CL = 16 | CL = 19 | tCK(AVG) | Reserved | | ns | 1,2,3,4,9 |
| | CL = 17 | CL = 20 | tCK(AVG) | 0.833 | <0.937 | ns | 1,2,3,4,9 |
| | | | | (Optional)[5,12] | | | 1,2,3,4,9 |
| | CL = 18 | CL = 21 | tCK(AVG) | 0.833 | <0.937 | ns | 1,2,3 |
| CWL = 14.18 | CL = 17 | CL = 20 | tCK(AVG) | Reserved | | ns | 1,2,3,4 |
| | CL = 18 | CL = 21 | tCK(AVG) | Reserved | | ns | 1,2,3,4 |
| | CL = 19 | CL = 22 | tCK(AVG) | 0.75 | <0.833 | ns | 1,2,3,4 |
| | CL = 20 | CL = 23 | tCK(AVG) | 0.75 | <0.833 | ns | 1,2,3 |
| Supported CL Settings | | | | 10,11,12,13,14,15,16,17,18,19,20 | | nCK | 12 |
| Supported CL Settings with read DBI | | | | 12,13,14,15,17,18,19,20,21,22,23 | | nCK | |
| Supported CWL Settings | | | | 9,10,11,12,14,16,18 | | nCK | |

## 10.1 Speed Bin Table Note

Absolute Specification
- VDDQ = VDD = 1.20V +/- 0.06 V
- VPP = 2.5V +0.25/-0.125 V
- The values defined with above-mentioned table are DLL ON case.
- DDR4-1600, 1866, 2133 and 2400 Speed Bin Tables are valid only when Gear_Down mode is disabled.

1. The CL setting and CWL setting result in tCK(avg).MIN and tCK(avg).MAX requirements. When making a selection of tCK(avg), both need to be fulfilled: Requirements from CL setting as well as requirements from CWL setting.
2. tCK(avg).MIN limits: Since CAS Latency is not purely analog - data and strobe output are synchronized by the DLL - all possible intermediate frequencies may not be guaranteed. CL in clock cycle is calculated from tAA following rounding algorithm defined in Section "Rounding Algorithms".
3. tCK(avg).MAX limits: Calculate tCK(avg) = tAA.MAX / CL SELECTED and round the resulting tCK(avg) down to the next valid speed bin (i.e. 1.5ns or 1.25ns or 1.071 ns or 0.937 ns or 0.833 ns). This result is tCK(avg).MAX corresponding to CL SELECTED.
4. 'Reserved' settings are not allowed. User must program a different value.
5. 'Optional' settings allow certain devices in the industry to support this setting, however, it is not a mandatory feature. Refer to supplier's data sheet and/or the DIMM SPD information if and how this setting is supported.
6. Any DDR4-1866 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/ Characterization.
7. Any DDR4-2133 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/ Characterization.
8. Any DDR4-2400 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/ Characterization.
9. Any DDR4-2666 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/ Characterization.
10. DDR4-1600 AC timing apply if DRAM operates at lower than 1600 MT/s data rate.
11. Parameters apply from tCK(avg)min to tCK(avg)max at all standard JEDEC clock period values as stated in the Speed Bin Tables.
12. CL number in parentheses, it means that these numbers are optional.
13. DDR4 SDRAM supports CL=9 as long as a system meets tAA(min).
14. Each speed bin lists the timing requirements that need to be supported in order for a given DRAM to be JEDEC compliant. JEDEC compliance does not require support for all speed bins within a given speed. JEDEC compliance requires meeting the parameters for a least one of the listed speed bins.

# 11. IDD and IDDQ Specification Parameters and Test Conditions

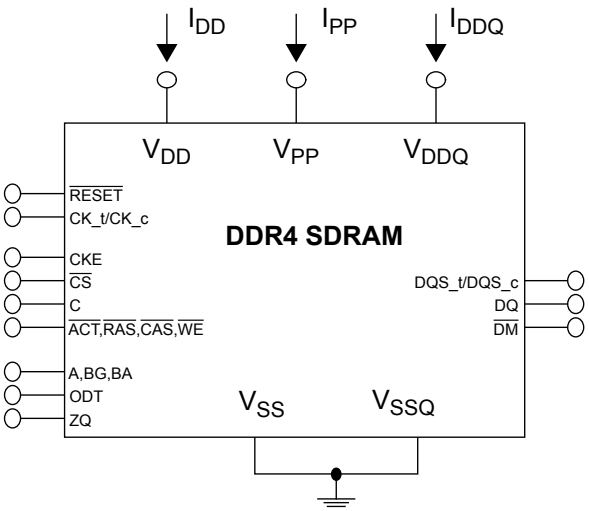
## 11.1 IDD, IPP and IDDQ Measurement Conditions

In this chapter, IDD, IPP and IDDQ measurement conditions such as test load and patterns are defined. Figure 21 shows the setup and test load for IDD, IPP and IDDQ measurements.

- IDD currents (such as IDD0, IDD0A, IDD1, IDD1A, IDD2N, IDD2NA, IDD2NL, IDD2NT, IDD2P, IDD2Q, IDD3N, IDD3NA, IDD3P, IDD4R, IDD4RA, IDD4W, IDD4WA, IDD5B, IDD5F2, IDD5F4, IDD6N, IDD6E, IDD6R, IDD6A, IDD7 and IDD8) are measured as time-averaged currents with all VDD balls of the DDR4 SDRAM under test tied together. Any IPP or IDDQ current is not included in IDD currents.
- IPP currents have the same definition as IDD except that the current on the VPP supply is measured.
- IDDQ currents (such as IDDQ2NT and IDDQ4R) are measured as time-averaged currents with all VDDQ balls of the DDR4 SDRAM under test tied together. Any IDD current is not included in IDDQ currents.
  Attention: IDDQ values cannot be directly used to calculate IO power of the DDR4 SDRAM. They can be used to support correlation of simulated IO power to actual IO power as outlined in Figure 22. In DRAM module application, IDDQ cannot be measured separately since VDD and VDDQ are using one merged-power layer in Module PCB.

For IDD, IPP and IDDQ measurements, the following definitions apply:

- “0” and “LOW” is defined as VIN <= $V_{ILAC(max)}$.
- “1” and “HIGH” is defined as VIN >= $V_{IHAC(min)}$.
- “MID-LEVEL” is defined as inputs are VREF = VDD / 2.
- Timings used for IDD, IPP and IDDQ Measurement-Loop Patterns are provided in Table 36.
- Basic IDD, IPP and IDDQ Measurement Conditions are described in Table 37.
- Detailed IDD, IPP and IDDQ Measurement-Loop Patterns are described in Table 38 through Table 46.
- IDD Measurements are done after properly initializing the DDR4 SDRAM. This includes but is not limited to setting
  RON = RZQ/7 (34 Ohm in MR1);
  RTT_NOM = RZQ/6 (40 Ohm in MR1);
  RTT_WR = RZQ/2 (120 Ohm in MR2);
  RTT_PARK = Disable;
  Qoff = $0_B$ (Output Buffer enabled) in MR1;
  TDQS_t disabled in MR1;
  CRC disabled in MR2;
  CA parity feature disabled in MR5;
  Gear down mode disabled in MR3
  Read/Write DBI disabled in MR5;
  DM disabled in MR5
- Attention: The IDD, IPP and IDDQ Measurement-Loop Patterns need to be executed at least one time before actual IDD or IDDQ measurement is started.
- Define D = {CS_n, ACT_n, RAS_n, CAS_n, WE_n } := {HIGH, LOW, LOW, LOW, LOW} ; apply BG/BA changes when directed.
- Define D# = {CS_n, ACT_n, RAS_n, CAS_n, WE_n } := {HIGH, HIGH, HIGH, HIGH, HIGH} apply invert of BG/BA changes when directed above.




**NOTE:**
1. DIMM level Output test load condition may be different from above

**Figure 21. Measurement Setup and Test Load for IDD, IPP and IDDQ Measurements**

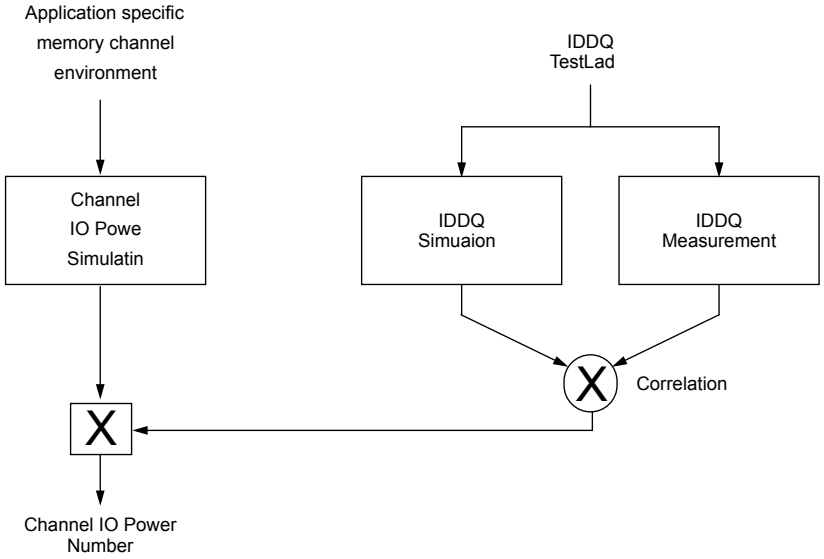



**Figure 22. Correlation from simulated Channel IO Power to actual Channel IO Power supported by IDDQ Measurement.**

**[ Table 36 ] Timings Used for IDD, IPP and IDDQ Measurement-Loop Patterns**

| Symbol | | DDR4-1600 | DDR4-1866 | DDR4-2133 | DDR4-2400 | DDR4-2666 | Unit |
|---|---|---|---|---|---|---|---|
| | | 11-11-11 | 13-13-13 | 15-15-15 | 17-17-17 | 19-19-19 | |
| tCK | | 1.25 | 1.071 | 0.937 | 0.833 | TBD | ns |
| CL | | 11 | 13 | 15 | 17 | TBD | nCK |
| CWL | | 11 | 12 | 14 | 16 | TBD | nCK |
| nRCD | | 11 | 13 | 15 | 17 | TBD | nCK |
| nRC | | 39 | 45 | 51 | 56 | TBD | nCK |
| nRAS | | 28 | 32 | 36 | 39 | TBD | nCK |
| nRP | | 11 | 13 | 15 | 17 | TBD | nCK |
| nFAW | x4 | 16 | 16 | 16 | 16 | TBD | nCK |
| | x8 | 20 | 22 | 23 | 26 | TBD | nCK |
| | x16 | 28 | 28 | 32 | 36 | TBD | nCK |
| nRRDS | x4 | 4 | 4 | 4 | 4 | TBD | nCK |
| | x8 | 4 | 4 | 4 | 4 | TBD | nCK |
| | x16 | 5 | 5 | 6 | 7 | TBD | nCK |
| nRRDL | x4 | 5 | 5 | 6 | 6 | TBD | nCK |
| | x8 | 5 | 5 | 6 | 6 | TBD | nCK |
| | x16 | 6 | 6 | 7 | 8 | TBD | nCK |
| tCCD_S | | 4 | 4 | 4 | 4 | TBD | nCK |
| tCCD_L | | 5 | 5 | 6 | 6 | TBD | nCK |
| tWTR_S | | 2 | 3 | 3 | 3 | TBD | nCK |
| tWTR_L | | 6 | 7 | 8 | 9 | TBD | nCK |
| nRFC 2Gb | | 128 | 150 | 171 | 193 | TBD | nCK |
| nRFC 4Gb | | 208 | 243 | 278 | 313 | TBD | nCK |
| nRFC 8Gb | | 280 | 327 | 374 | 421 | TBD | nCK |
| TBD | | | | | | | nCK |

**[ Table 37 ] Basic IDD, IPP and IDDQ Measurement Conditions**

| Symbol | Description |
|---|---|
| IDD0 | **Operating One Bank Active-Precharge Current (AL=0)**<br>**CKE:** High; **External clock:** On; **tCK, nRC, nRAS, CL**: see Table 36 on page 42; **BL:** 8[1]; **AL:** 0; **CS_n:** High between ACT and PRE; **Command, Address, Bank Group Address, Bank Address Inputs:** partially toggling according to Table 38 on page 46; **Data IO:** VDDQ; **DM_n:** stable at 1; **Bank Activity:** Cycling with one bank active at a time: 0,0,1,1,2,2,... (see Table 38 on page 46); **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0; **Pattern Details:** see Table 38 on page 46 |
| IDD0A | **Operating One Bank Active-Precharge Current (AL=CL-1)**<br>**AL = CL-1, Other conditions:** see IDD0 |
| IPP0 | **Operating One Bank Active-Precharge IPP Current**<br>**Same condition with IDD0** |
| IDD1 | **Operating One Bank Active-Read-Precharge Current (AL=0)**<br>**CKE:** High; **External clock:** On; **tCK, nRC, nRAS, nRCD, CL**: see Table 36 on page 42; **BL:** 8[1]; **AL:** 0; **CS_n**: High between ACT, RD and PRE; **Command, Address, Bank Group Address, Bank Address Inputs, Data IO:** partially toggling according to Table 39 on page 47; **DM_n:** stable at 1; **Bank Activity:** Cycling with one bank active at a time: 0,0,1,1,2,2,... (see Table 39 on page 47); **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0; **Pattern Details:** see Table 39 on page 47 |
| IDD1A | **Operating One Bank Active-Read-Precharge Current (AL=CL-1)**<br>**AL = CL-1, Other conditions:** see IDD1 |
| IPP1 | **Operating One Bank Active-Read-Precharge IPP Current**<br>**Same condition with IDD1** |
| IDD2N | **Precharge Standby Current (AL=0)**<br>**CKE**: High; **External clock:** On; **tCK, CL**: see Table 36 on page 42; **BL:** 8[1]; **AL:** 0; **CS_n**: stable at 1; **Command, Address, Bank Group Address, Bank Address Inputs:** partially toggling according to Table 40 on page 48; **Data IO:** VDDQ; **DM_n:** stable at 1; **Bank Activity:** all banks closed; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0; **Pattern Details:** see Table 40 on page 48 |
| IDD2NA | **Precharge Standby Current (AL=CL-1)**<br>**AL = CL-1, Other conditions:** see IDD2N |
| IPP2N | **Precharge Standby IPP Current**<br>**Same condition with IDD2N** |
| IDD2NT | **Precharge Standby ODT Current**<br>**CKE**: High; **External clock:** On; **tCK, CL**: see Table 36 on page 42; **BL:** 8[1]; **AL:** 0; **CS_n**: stable at 1; **Command, Address, Bank Group Address, Bank Address Inputs:** partially toggling according to Table 41 on page 49; **Data IO: VSSQ**; **DM_n:** stable at 1; **Bank Activity:** all banks closed; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** toggling according to Table 41 on page 49; **Pattern Details:** see Table 41 on page 49 |
| IDDQ2NT (Optional) | **Precharge Standby ODT IDDQ Current**<br>Same definition like for IDD2NT, however measuring IDDQ current instead of IDD current |
| IDD2NL | **Precharge Standby Current with CAL enabled**<br>Same definition like for IDD2N, CAL enabled[3] |
| IDD2NG | **Precharge Standby Current with Gear Down mode enabled**<br>Same definition like for IDD2N, Gear Down mode enabled[3,5] |
| IDD2ND | **Precharge Standby Current with DLL disabled**<br>Same definition like for IDD2N, DLL disabled[3] |
| IDD2N_par | **Precharge Standby Current with CA parity enabled**<br>Same definition like for IDD2N, CA parity enabled[3] |
| IDD2P | **Precharge Power-Down Current CKE:** Low; **External clock:** On; **tCK, CL**: see Table 36 on page 42; **BL:** 8[1]; **AL:** 0; **CS_n**: stable at 1; **Command, Address, Bank Group Address, Bank Address Inputs:** stable at 0; **Data IO:** VDDQ; **DM_n:** stable at 1; **Bank Activity:** all banks closed; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0 |
| IPP2P | **Precharge Power-Down IPP Current**<br>**Same condition with IDD2P** |
| IDD2Q | **Precharge Quiet Standby Current**<br>**CKE**: High; **External clock:** On; **tCK, CL**: see Table 36 on page 42; **BL:** 8[1]; **AL:** 0; **CS_n**: stable at 1; **Command, Address, Bank Group Address, Bank Address Inputs:** stable at 0; **Data IO:** VDDQ; **DM_n:** stable at 1;**Bank Activity:** all banks closed; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0 |
| IDD3N | **Active Standby Current**<br>**CKE**: High; **External clock:** On; **tCK, CL**: see Table 36 on page 42; **BL:** 8[1]; **AL:** 0; **CS_n**: stable at 1; **Command, Address, Bank Group Address, Bank Address Inputs:** partially toggling according to Table 40 on page 48; **Data IO:** VDDQ; **DM_n:** stable at 1;**Bank Activity:** all banks open; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0; **Pattern Details:** see Table 40 on page 48 |

| Symbol | Description |
|---|---|
| IDD3NA | **Active Standby Current (AL=CL-1)**<br>**AL = CL-1, Other conditions:** see IDD3N |
| IPP3N | **Active Standby IPP Current**<br>**Same condition with IDD3N** |
| IDD3P | **Active Power-Down Current**<br>**CKE:** Low; **External clock:** On; **tCK, CL**: see Table 36 on page 42; **BL:** 8[1]; **AL:** 0; **CS_n**: stable at 1; **Command, Address, Bank Group Address, Bank Address Inputs:** stable at 0; **Data IO:** VDDQ; **DM_n:** stable at 1; **Bank Activity:** all banks open; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0 |
| IPP3P | **Active Power-Down IPP Current**<br>**Same condition with IDD3P** |
| IDD4R | **Operating Burst Read Current**<br>**CKE:** High; **External clock:** On; **tCK, CL**: see Table 36 on page 42; **BL:** 8[2]; **AL:** 0; **CS_n**: High between RD; **Command, Address, Bank Group Address, Bank Address Inputs:** partially toggling according to Table 42 on page 50; **Data IO:** seamless read data burst with different data between one burst and the next one according to Table 42 on page 50; **DM_n**: stable at 1; **Bank Activity:** all banks open, RD commands cycling through banks: 0,0,1,1,2,2,... (see Table 42 on page 50); **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0; **Pattern Details:** see Table 42 on page 50 |
| IDD4RA | **Operating Burst Read Current (AL=CL-1)**<br>**AL = CL-1, Other conditions:** see IDD4R |
| IDD4RB | **Operating Burst Read Current with Read DBI**<br>**Read DBI enabled[3], Other conditions:** see IDD4R |
| IPP4R | **Operating Burst Read IPP Current**<br>**Same condition with IDD4R** |
| IDDQ4R (Optional) | **Operating Burst Read IDDQ Current**<br>Same definition like for IDD4R, however measuring IDDQ current instead of IDD current |
| IDDQ4RB (Optional) | **Operating Burst Read IDDQ Current with Read DBI**<br>Same definition like for IDD4RB, however measuring IDDQ current instead of IDD current |
| IDD4W | **Operating Burst Write Current**<br>**CKE:** High; **External clock:** On; **tCK, CL**: see Table 36 on page 42; **BL:** 8[1]; **AL:** 0; **CS_n**: High between WR; **Command, Address, Bank Group Address, Bank Address Inputs:** partially toggling according to Table 43 on page 51; **Data IO:** seamless write data burst with different data between one burst and the next one according to Table 43 on page 51; **DM_n:** stable at 1; **Bank Activity:** all banks open, WR commands cycling through banks: 0,0,1,1,2,2,... (see Table 43 on page 51); **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at HIGH; **Pattern Details:** see Table 43 on page 51 |
| IDD4WA | **Operating Burst Write Current (AL=CL-1)**<br>**AL = CL-1, Other conditions:** see IDD4W |
| IDD4WB | **Operating Burst Write Current with Write DBI**<br>**Write DBI enabled[3], Other conditions:** see IDD4W |
| IDD4WC | **Operating Burst Write Current with Write CRC**<br>**Write CRC enabled[3], Other conditions:** see IDD4W |
| IDD4W_par | **Operating Burst Write Current with CA Parity**<br>**CA Parity enabled[3], Other conditions:** see IDD4W |
| IPP4W | **Operating Burst Write IPP Current**<br>**Same condition with IDD4W** |
| IDD5B | **Burst Refresh Current (1X REF)**<br>**CKE:** High; **External clock:** On; **tCK, CL, nRFC**: see Table 36 on page 42; **BL:** 8[1]; **AL:** 0; **CS_n**: High between REF; **Command, Address, Bank Group Address, Bank Address Inputs:** partially toggling according to Table 45 on page 53; **Data IO:** VDDQ; **DM_n:** stable at 1; **Bank Activity:** REF command every nRFC (see Table 45 on page 53); **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0; **Pattern Details:** see Table 45 on page 53 |
| IPP5B | **Burst Refresh Write IPP Current (1X REF)**<br>**Same condition with IDD5B** |
| IDD5F2 | **Burst Refresh Current (2X REF)**<br>**tRFC=tRFC_x2, Other conditions:** see IDD5B |
| IPP5F2 | **Burst Refresh Write IPP Current (2X REF)**<br>**Same condition with IDD5F2** |
| IDD5F4 | **Burst Refresh Current (4X REF)**<br>**tRFC=tRFC_x4, Other conditions:** see IDD5B |
| IPP5F4 | **Burst Refresh Write IPP Current (4X REF)**<br>**Same condition with IDD5F4** |

| Symbol | Description |
|---|---|
| IDD6N | **Self Refresh Current: Normal Temperature Range**<br>**$T_{CASE}$:** 0 - 85°C; **Low Power Array Self Refresh (LP ASR)** : Normal[4]; **CKE:** Low; **External clock:** Off; CK_t and CK_c#: LOW; **CL**: see Table 36 on page 42; **BL:** 8[1]; **AL:** 0; **CS_n#, Command, Address, Bank Group Address, Bank Address, Data IO:** High; **DM_n:** stable at 1; **Bank Activity:** Self-Refresh operation; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** MID-LEVEL |
| IPP6N | **Self Refresh IPP Current: Normal Temperature Range**<br>**Same condition with IDD6N** |
| IDD6E | **Self-Refresh Current: Extended Temperature Range**)<br>**$T_{CASE}$:** 0 - 95°C; **Low Power Array Self Refresh (LP ASR)** : Extended[4]; **CKE:** Low; **External clock:** Off; CK_t and CK_c: LOW; **CL**: see Table 36 on page 42; **BL:** 8[1]; **AL:** 0; **CS_n, Command, Address, Bank Group Address, Bank Address, Data IO:** High; **DM_n**:stable at 1; **Bank Activity:** Extended Temperature Self-Refresh operation; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** MID-LE**VEL** |
| IPP6E | **Self Refresh IPP Current: Extended Temperature Range**<br>**Same condition with IDD6E** |
| IDD6R | **Self-Refresh Current: Reduced Temperature Range**<br>**$T_{CASE}$:** 0 - 45 °C; **Low Power Array Self Refresh (LP ASR)** : Reduced[4]; **CKE:** Low; **External clock:** Off; CK_t and CK_c#: LOW; **CL**: see Table 36 on page 42; **BL:** 8[1]; **AL:** 0; **CS_n#, Command, Address, Bank Group Address, Bank Address, Data IO:** High; **DM_n**:stable at 1; **Bank Activity:** Extended Temperature Self-Refresh operation; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** MID-LEVEL |
| IPP6R | **Self Refresh IPP Current: Reduced Temperature Range**<br>**Same condition with IDD6R** |
| IDD6A | **Auto Self-Refresh Current**<br>**$T_{CASE}$:** 0 - 95°C; **Low Power Array Self Refresh (LP ASR)** : Auto[4];**CKE:** Low; **External clock:** Off; CK_t and CK_c#: LOW; **CL**: see Table 36 on page 42; **BL:** 8[1]; **AL:** 0; **CS_n#, Command, Address, Bank Group Address, Bank Address, Data IO:** High; **DM_n**:stable at 1; **Bank Activity:** Auto Self-Refresh operation; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** MID-LEVEL |
| IPP6A | **Auto Self-Refresh IPP Current**<br>**Same condition with IDD6A** |
| IDD7 | **Operating Bank Interleave Read Current**<br>**CKE:** High; **External clock:** On; **tCK, nRC, nRAS, nRCD, nRRD, nFAW, CL**: see Table 36 on page 42; **BL:** 8[1]; **AL:** CL-1; **CS_n**: High between ACT and RDA; **Command, Address, Bank Group Address, Bank Address Inputs:** partially toggling according to Table 46 on page 54; **Data IO:** read data bursts with different data between one burst and the next one according to Table 46 on page 54; **DM_n:** stable at 1; **Bank Activity:** two times interleaved cycling through banks (0, 1, ...7) with different addressing, see Table 46 on page 54; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0; **Pattern Details:** see Table 46 on page 54 |
| IPP7 | **Operating Bank Interleave Read IPP Current**<br>**Same condition with IDD7** |
| IDD8 | **Maximum Power Down Current**<br>**TBD** |
| IPP8 | **Maximum Power Down IPP Current**<br>**Same condition with IDD8** |

**NOTE :**
1. Burst Length: BL8 fixed by MRS: set MR0 [A1:0=00].
2. Output Buffer Enable
   - set MR1 [A12 = 0] : Qoff = Output buffer enabled
   - set MR1 [A2:1 = 00] : Output Driver Impedance Control = RZQ/7
   RTT_Nom enable
   - set MR1 [A10:8 = 011] : RTT_NOM = RZQ/6
   RTT_WR enable
   - set MR2 [A10:9 = 01] : RTT_WR = RZQ/2
   RTT_PARK disable
   - set MR5 [A8:6 = 000]
3. CAL enabled : set MR4 [A8:6 = 001] : 1600MT/s
   010] : 1866MT/s, 2133MT/s
   011] : 2400MT/s, 2666MT/s
   Gear Down mode enabled :set MR3 [A3 = 1] : 1/4 Rate
   DLL disabled : set MR1 [A0 = 0]
   CA parity enabled :set MR5 [A2:0 = 001] : 1600MT/s,1866MT/s, 2133MT/s
   010] : 2400MT/s, 2666MT/s
   Read DBI enabled : set MR5 [A12 = 1]
   Write DBI enabled : set :MR5 [A11 = 1]
4. Low Power Auto Self Refresh (LP ASR) : set MR2 [A7:6 = 00] : Normal
   01] : Reduced Temperature range
   10] : Extended Temperature range
   11] : Auto Self Refresh
5. IDD2NG should be measured after sync pulse(NOP) input.

**[ Table 38 ] IDD0, IDD0A and IPP0 Measurement-Loop Pattern[1]**

| CK_t /CK_c | CKE | Sub-Loop | Cycle Number | Command | CS_n | ACT_n | RAS_n | CAS_n/ A15 | WE_n/ A14 | ODT | C[2:0][3] | BG[1:0][2] | BA[1:0] | A12/BC_n | A[13,11] | A[10]/AP | A[9:7] | A[6:3] | A[2:0] | Data[4] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| toggling | Static High | 0 | 0 | **ACT** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | - |
| | | | 1,2 | D, D | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | - |
| | | | 3,4 | D_#, D_# | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 3[2] | 3 | 0 | 0 | 0 | 7 | F | 0 | - |
| | | | ... | repeat pattern 1...4 until nRAS - 1, truncate if necessary | | | | | | | | | | | | | | | | |
| | | | nRAS | PRE | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | - |
| | | | ... | repeat pattern 1...4 until nRC - 1, truncate if necessary | | | | | | | | | | | | | | | | |
| | | 1 | 1*nRC | repeat Sub-Loop 0, use **BG[1:0][2] = 1, BA[1:0] = 1** instead | | | | | | | | | | | | | | | | |
| | | 2 | 2*nRC | repeat Sub-Loop 0, use **BG[1:0][2] = 0, BA[1:0] = 2** instead | | | | | | | | | | | | | | | | |
| | | 3 | 3*nRC | repeat Sub-Loop 0, use **BG[1:0][2] = 1, BA[1:0] = 3** instead | | | | | | | | | | | | | | | | |
| | | 4 | 4*nRC | repeat Sub-Loop 0, use **BG[1:0][2] = 0, BA[1:0] = 1** instead | | | | | | | | | | | | | | | | |
| | | 5 | 5*nRC | repeat Sub-Loop 0, use **BG[1:0][2] = 1, BA[1:0] = 2** instead | | | | | | | | | | | | | | | | |
| | | 6 | 6*nRC | repeat Sub-Loop 0, use **BG[1:0][2] = 0, BA[1:0] = 3** instead | | | | | | | | | | | | | | | | |
| | | 7 | 7*nRC | repeat Sub-Loop 0, use **BG[1:0][2] = 1, BA[1:0] = 0** instead | | | | | | | | | | | | | | | | |
| | | 8 | 8*nRC | repeat Sub-Loop 0, use **BG[1:0][2] = 2, BA[1:0] = 0** instead | | | | | | | | | | | | | | | | For x4 and x8 only |
| | | 9 | 9*nRC | repeat Sub-Loop 0, use **BG[1:0][2] = 3, BA[1:0] = 1** instead | | | | | | | | | | | | | | | | |
| | | 10 | 10*nRC | repeat Sub-Loop 0, use **BG[1:0][2] = 2, BA[1:0] = 2** instead | | | | | | | | | | | | | | | | |
| | | 11 | 11*nRC | repeat Sub-Loop 0, use **BG[1:0][2] = 3, BA[1:0] = 3** instead | | | | | | | | | | | | | | | | |
| | | 12 | 12*nRC | repeat Sub-Loop 0, use **BG[1:0][2] = 2, BA[1:0] = 1** instead | | | | | | | | | | | | | | | | |
| | | 13 | 13*nRC | repeat Sub-Loop 0, use **BG[1:0][2] = 3, BA[1:0] = 2** instead | | | | | | | | | | | | | | | | |
| | | 14 | 14*nRC | repeat Sub-Loop 0, use **BG[1:0][2] = 2, BA[1:0] = 3** instead | | | | | | | | | | | | | | | | |
| | | 15 | 15*nRC | repeat Sub-Loop 0, use **BG[1:0][2] = 3, BA[1:0] = 0** instead | | | | | | | | | | | | | | | | |

**NOTE :**
1. DQS_t, DQS_c are VDDQ.
2. BG1 is don't care for x16 device
3. C[2:0] are used only for 3DS device
4. DQ signals are VDDQ.

**[ Table 39 ] IDD1, IDD1A and IPP1 Measurement-Loop Pattern[1]**

| CK_t, CK_c | CKE | Sub-Loop | Cycle Number | Command | CS_n | ACT_n | RAS_n | CAS_n/A15 | WE_n/A14 | ODT | C[2:0][3] | BG[1:0][2] | BA[1:0] | A12/BC_n | A[13,11] | A[10]/AP | A[9:7] | A[6:3] | A[2:0] | Data[4] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| toggling | Static High | 0 | 0 | **ACT** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | **0** | **0** | 0 | 0 | 0 | 0 | 0 | - |
| | | | 1, 2 | D, D | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | **0** | **0** | 0 | 0 | 0 | 0 | 0 | - |
| | | | 3, 4 | D#, D# | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 3[b] | **3** | **0** | 0 | 0 | 7 | F | 0 | - |
| | | | ... | repeat pattern 1...4 until nRCD - AL - 1, truncate if necessary | | | | | | | | | | | | | | | | |
| | | | nRCD -AL | **RD** | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | **D0=00, D1=FF D2=FF, D3=00 D4=FF, D5=00 D6=00, D7=FF** |
| | | | ... | repeat pattern 1...4 until nRAS - 1, truncate if necessary | | | | | | | | | | | | | | | | |
| | | | nRAS | **PRE** | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | **0** | **0** | 0 | 0 | 0 | 0 | 0 | - |
| | | | ... | repeat pattern 1...4 until nRC - 1, truncate if necessary | | | | | | | | | | | | | | | | |
| | | 1 | 1*nRC + 0 | **ACT** | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | **1** | **0** | 0 | 0 | 0 | 0 | 0 | - |
| | | | 1*nRC + 1, 2 | D, D | 1 | 0 | 0 | 0 | 0 | 0 | **0** | **0** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | - |
| | | | 1*nRC + 3, 4 | D#, D# | 1 | 1 | 1 | 1 | 1 | 0 | **0** | 3[b] | **3** | **0** | 0 | 0 | 7 | F | 0 | - |
| | | | ... | repeat pattern nRC + 1...4 until 1*nRC + nRAS - 1, truncate if necessary | | | | | | | | | | | | | | | | |
| | | | 1*nRC + nRCD - AL | **RD** | 0 | 1 | 1 | 0 | 1 | 0 | **0** | **1** | 1 | 0 | 0 | 0 | 0 | **0** | **0** | **D0=FF, D1=00 D2=00, D3=FF D4=00, D5=FF D6=FF, D7=00** |
| | | | ... | repeat pattern 1...4 until nRAS - 1, truncate if necessary | | | | | | | | | | | | | | | | |
| | | | 1*nRC + nRAS | **PRE** | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | **0** | **0** | 0 | 0 | 0 | 0 | 0 | - |
| | | | ... | repeat nRC + 1...4 until 2*nRC - 1, truncate if necessary | | | | | | | | | | | | | | | | |
| | | 2 | 2*nRC | repeat Sub-Loop 0, use **BG[1:0][2] = 0, BA[1:0] = 2** instead | | | | | | | | | | | | | | | | |
| | | 3 | 3*nRC | repeat Sub-Loop 1, use **BG[1:0][2] = 1, BA[1:0] = 3** instead | | | | | | | | | | | | | | | | |
| | | 4 | 4*nRC | repeat Sub-Loop 0, use **BG[1:0][2] = 0, BA[1:0] = 1** instead | | | | | | | | | | | | | | | | |
| | | 5 | 5*nRC | repeat Sub-Loop 1, use **BG[1:0][2] = 1, BA[1:0] = 2** instead | | | | | | | | | | | | | | | | |
| | | 6 | 6*nRC | repeat Sub-Loop 0, use **BG[1:0][2] = 0, BA[1:0] = 3** instead | | | | | | | | | | | | | | | | |
| | | 8 | 7*nRC | repeat Sub-Loop 1, use **BG[1:0][2] = 1, BA[1:0] = 0** instead | | | | | | | | | | | | | | | | |
| | | 9 | 9*nRC | repeat Sub-Loop 1, use **BG[1:0][2] = 2, BA[1:0] = 0** instead | | | | | | | | | | | | | | | | For x4 and x8 only |
| | | 10 | 10*nRC | repeat Sub-Loop 0, use **BG[1:0][2] = 3, BA[1:0] = 1** instead | | | | | | | | | | | | | | | | |
| | | 11 | 11*nRC | repeat Sub-Loop 1, use **BG[1:0][2] = 2, BA[1:0] = 2** instead | | | | | | | | | | | | | | | | |
| | | 12 | 12*nRC | repeat Sub-Loop 0, use **BG[1:0][2] = 3, BA[1:0] = 3** instead | | | | | | | | | | | | | | | | |
| | | 13 | 13*nRC | repeat Sub-Loop 1, use **BG[1:0][2] = 2, BA[1:0] = 1** instead | | | | | | | | | | | | | | | | |
| | | 14 | 14*nRC | repeat Sub-Loop 0, use **BG[1:0][2] = 3, BA[1:0] =** 2 instead | | | | | | | | | | | | | | | | |
| | | 15 | 15*nRC | repeat Sub-Loop 1, use **BG[1:0][2] = 2, BA[1:0] =** 3 instead | | | | | | | | | | | | | | | | |
| | | 16 | 16*nRC | repeat Sub-Loop 0, use **BG[1:0][2] = 3, BA[1:0] =** 0 instead | | | | | | | | | | | | | | | | |

**NOTE :**
1. DQS_t, DQS_c are used according to RD Commands, otherwise VDDQ
2. BG1 is don't care for x16 device
3. C[2:0] are used only for 3DS device
4. Burst Sequence driven on each DQ signal by Read Command. Outside burst operation, DQ signals are VDDQ.

**[ Table 40 ] IDD2N, IDD2NA, IDD2NL, IDD2NG, IDD2ND, IDD2N_par, IPP2,IDD3N, IDD3NA and IDD3P Measurement-Loop Pattern[1]**

| CK_t, CK_c | CKE | Sub-Loop | Cycle Number | Command | CS_n | ACT_n | RAS_n | CAS_n/A15 | WE_n/A14 | ODT | C[2:0][3] | BG[1:0][2] | BA[1:0] | A12/BC_n | A[13,11] | A[10]/AP | A[9:7] | A[6:3] | A[2:0] | Data[4] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| toggling | Static High | 0 | 0 | D, D | 1 | 0 | 0 | 0 | 0 | 0 | 0 | **0** | **0** | 0 | 0 | 0 | **0** | **0** | 0 | 0 |
| | | | 1 | D, D | 1 | 0 | 0 | 0 | 0 | 0 | 0 | **0** | **0** | 0 | 0 | 0 | **0** | **0** | 0 | 0 |
| | | | 2 | D#, D# | 1 | 1 | 1 | 1 | 1 | 0 | 0 | **3**[2] | **3** | 0 | 0 | 0 | **7** | **F** | 0 | 0 |
| | | | 3 | D#, D# | 1 | 1 | 1 | 1 | 1 | 0 | 0 | **3**[2] | **3** | 0 | 0 | 0 | **7** | **F** | 0 | 0 |
| | | 1 | 4-7 | repeat Sub-Loop 0, use **BG[1:0]**[2] **= 1, BA[1:0] = 1** instead | | | | | | | | | | | | | | | | |
| | | 2 | 8-11 | repeat Sub-Loop 0, use **BG[1:0]**[2] **= 0, BA[1:0] = 2** instead | | | | | | | | | | | | | | | | |
| | | 3 | 12-15 | repeat Sub-Loop 0, use **BG[1:0]**[2] **= 1, BA[1:0] = 3** instead | | | | | | | | | | | | | | | | |
| | | 4 | 16-19 | repeat Sub-Loop 0, use **BG[1:0]**[2] **= 0, BA[1:0] = 1** instead | | | | | | | | | | | | | | | | |
| | | 5 | 20-23 | repeat Sub-Loop 0, use **BG[1:0]**[2] **= 1, BA[1:0] = 2** instead | | | | | | | | | | | | | | | | |
| | | 6 | 24-27 | repeat Sub-Loop 0, use **BG[1:0]**[2] **= 0, BA[1:0] = 3** instead | | | | | | | | | | | | | | | | |
| | | 7 | 28-31 | repeat Sub-Loop 0, use **BG[1:0]**[2] **= 1, BA[1:0] = 0** instead | | | | | | | | | | | | | | | | |
| | | 8 | 32-35 | repeat Sub-Loop 0, use **BG[1:0]**[2] **= 2, BA[1:0] = 0** instead | | | | | | | | | | | | | | | | |
| | | 9 | 36-39 | repeat Sub-Loop 0, use **BG[1:0]**[2] **= 3, BA[1:0] = 1** instead | | | | | | | | | | | | | | | | |
| | | 10 | 40-43 | repeat Sub-Loop 0, use **BG[1:0]**[2] **= 2, BA[1:0] = 2** instead | | | | | | | | | | | | | | | | |
| | | 11 | 44-47 | repeat Sub-Loop 0, use **BG[1:0]**[2] **= 3, BA[1:0] = 3** instead | | | | | | | | | | | | | | | | |
| | | 12 | 48-51 | repeat Sub-Loop 0, use **BG[1:0]**[2] **= 2, BA[1:0] = 1** instead | | | | | | | | | | | | | | | | |
| | | 13 | 52-55 | repeat Sub-Loop 0, use **BG[1:0]**[2] **= 3, BA[1:0] = 2** instead | | | | | | | | | | | | | | | | |
| | | 14 | 56-59 | repeat Sub-Loop 0, use **BG[1:0]**[2] **= 2, BA[1:0] = 3** instead | | | | | | | | | | | | | | | | |
| | | 15 | 60-63 | repeat Sub-Loop 0, use **BG[1:0]**[2] **= 3, BA[1:0] = 0** instead | | | | | | | | | | | | | | | | |

**NOTE :**
1. DQS_t, DQS_c are VDDQ.
2. BG1 is don't care for x16 device
3. C[2:0] are used only for 3DS device
4. DQ signals are VDDQ.

**[ Table 41 ] IDD2NT and IDDQ2NT Measurement-Loop Pattern[1]**

| CK_t, CK_c | CKE | Sub-Loop | Cycle Number | Command | CS_n | ACT_n | RAS_n | CAS_n/A15 | WE_n/A14 | ODT | C[2:0][3] | BG[1:0][2] | BA[1:0] | A12/BC_n | A[13,11] | A[10]/AP | A[9:7] | A[6:3] | A[2:0] | Data[4] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| toggling | Static High | 0 | 0 | D, D | 1 | 0 | 0 | 0 | 0 | 0 | 0 | **0** | **0** | 0 | 0 | 0 | **0** | **0** | 0 | - |
| | | | 1 | D, D | 1 | 0 | 0 | 0 | 0 | 0 | 0 | **0** | **0** | 0 | 0 | 0 | **0** | **0** | 0 | - |
| | | | 2 | D#, D# | 1 | 1 | 1 | 1 | 1 | 0 | 0 | **3**[2] | **3** | 0 | 0 | 0 | **7** | **F** | 0 | - |
| | | | 3 | D#, D# | 1 | 1 | 1 | 1 | 1 | 0 | 0 | **3**[2] | **3** | 0 | 0 | 0 | **7** | **F** | 0 | - |
| | | 1 | 4-7 | repeat Sub-Loop 0, but ODT = 1 and **BG[1:0][2] = 1, BA[1:0] = 1** instead | | | | | | | | | | | | | | | | |
| | | 2 | 8-11 | repeat Sub-Loop 0, but ODT = 0 and **BG[1:0][2] = 0, BA[1:0] = 2** instead | | | | | | | | | | | | | | | | |
| | | 3 | 12-15 | repeat Sub-Loop 0, but ODT = 1 and **BG[1:0][2] = 1, BA[1:0] = 3** instead | | | | | | | | | | | | | | | | |
| | | 4 | 16-19 | repeat Sub-Loop 0, but ODT = 0 and **BG[1:0][2] = 0, BA[1:0] = 1** instead | | | | | | | | | | | | | | | | |
| | | 5 | 20-23 | repeat Sub-Loop 0, but ODT = 1 and **BG[1:0][2] = 1, BA[1:0] = 2** instead | | | | | | | | | | | | | | | | |
| | | 6 | 24-27 | repeat Sub-Loop 0, but ODT = 0 and **BG[1:0][2] = 0, BA[1:0] = 3** instead | | | | | | | | | | | | | | | | |
| | | 7 | 28-31 | repeat Sub-Loop 0, but ODT = 1 and **BG[1:0][2] = 1, BA[1:0] = 0** instead | | | | | | | | | | | | | | | | |
| | | 8 | 32-35 | repeat Sub-Loop 0, but ODT = 0 and **BG[1:0][2] = 2, BA[1:0] = 0** instead | | | | | | | | | | | | | | | | For x4 and x8 only |
| | | 9 | 36-39 | repeat Sub-Loop 0, but ODT = 1 and **BG[1:0][2] = 3, BA[1:0] = 1** instead | | | | | | | | | | | | | | | | |
| | | 10 | 40-43 | repeat Sub-Loop 0, but ODT = 0 and **BG[1:0][2] = 2, BA[1:0] = 2** instead | | | | | | | | | | | | | | | | |
| | | 11 | 44-47 | repeat Sub-Loop 0, but ODT = 1 and **BG[1:0][2] = 3, BA[1:0] = 3** instead | | | | | | | | | | | | | | | | |
| | | 12 | 48-51 | repeat Sub-Loop 0, but ODT = 0 and **BG[1:0][2] = 2, BA[1:0] = 1** instead | | | | | | | | | | | | | | | | |
| | | 13 | 52-55 | repeat Sub-Loop 0, but ODT = 1 and **BG[1:0][2] = 3, BA[1:0] = 2** instead | | | | | | | | | | | | | | | | |
| | | 14 | 56-59 | repeat Sub-Loop 0, but ODT = 0 and **BG[1:0][2] = 2, BA[1:0] = 3** instead | | | | | | | | | | | | | | | | |
| | | 15 | 60-63 | repeat Sub-Loop 0, but ODT = 1 and **BG[1:0][2] = 3, BA[1:0] = 0** instead | | | | | | | | | | | | | | | | |

**NOTE :**
1. DQS_t, DQS_c are VDDQ.
2. BG1 is don't care for x16 device
3. C[2:0] are used only for 3DS device
4. DQ signals are VDDQ.

**[ Table 42 ] IDD4R, IDDR4RA, IDD4RB and IDDQ4R Measurement-Loop Pattern[1]**

| CK_t, CK_c | CKE | Sub-Loop | Cycle Number | Command | CS_n | ACT_n | RAS_n | CAS_n/A15 | WE_n/A14 | ODT | C[2:0][3] | BG[1:0][2] | BA[1:0] | A12/BC_n | A[13,11] | A[10]/AP | A[9:7] | A[6:3] | A[2:0] | Data[4] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| toggling | Static High | 0 | 0 | **RD** | 0 | 1 | 1 | 0 | 1 | 0 | 0 | **0** | **0** | 0 | 0 | 0 | **0** | **0** | 0 | **D0=00, D1=FF<br>D2=FF, D3=00<br>D4=FF, D5=00<br>D6=00, D7=FF** |
| | | | 1 | D | 1 | 0 | 0 | 0 | 0 | 0 | 0 | **0** | **0** | 0 | 0 | 0 | **0** | **0** | 0 | - |
| | | | 2,3 | D#, D# | 1 | 1 | 1 | 1 | 1 | 0 | 0 | **3**[2] | **3** | 0 | 0 | 0 | **7** | **F** | 0 | - |
| | | 1 | 4 | **RD** | 0 | 1 | 1 | 0 | 1 | 0 | 0 | **1** | **1** | 0 | 0 | 0 | **7** | **F** | 0 | **D0=FF, D1=00<br>D2=00, D3=FF<br>D4=00, D5=FF<br>D6=FF, D7=00** |
| | | | 5 | D | 1 | 0 | 0 | 0 | 0 | 0 | 0 | **0** | **0** | 0 | 0 | 0 | **0** | **0** | 0 | - |
| | | | 6,7 | D#, D# | 1 | 1 | 1 | 1 | 1 | 0 | 0 | **3**[2] | **3** | 0 | 0 | 0 | **7** | **F** | 0 | - |
| | | 2 | 8-11 | repeat Sub-Loop 0, use **BG[1:0]**[2] **= 0, BA[1:0] = 2** instead | | | | | | | | | | | | | | | | |
| | | 3 | 12-15 | repeat Sub-Loop 1, use **BG[1:0]**[2] **= 1, BA[1:0] = 3** instead | | | | | | | | | | | | | | | | |
| | | 4 | 16-19 | repeat Sub-Loop 0, use **BG[1:0]**[2] **= 0, BA[1:0] = 1** instead | | | | | | | | | | | | | | | | |
| | | 5 | 20-23 | repeat Sub-Loop 1, use **BG[1:0]**[2] **= 1, BA[1:0] = 2** instead | | | | | | | | | | | | | | | | |
| | | 6 | 24-27 | repeat Sub-Loop 0, use **BG[1:0]**[2] **= 0, BA[1:0] = 3** instead | | | | | | | | | | | | | | | | |
| | | 7 | 28-31 | repeat Sub-Loop 1, use **BG[1:0]**[2] **= 1, BA[1:0] = 0** instead | | | | | | | | | | | | | | | | |
| | | 8 | 32-35 | repeat Sub-Loop 0, use **BG[1:0]**[2] **= 2, BA[1:0] = 0** instead | | | | | | | | | | | | | | | | For x4 and x8 only |
| | | 9 | 36-39 | repeat Sub-Loop 1, use **BG[1:0]**[2] **= 3, BA[1:0] = 1** instead | | | | | | | | | | | | | | | | |
| | | 10 | 40-43 | repeat Sub-Loop 0, use **BG[1:0]**[2] **= 2, BA[1:0] = 2** instead | | | | | | | | | | | | | | | | |
| | | 11 | 44-47 | repeat Sub-Loop 1, use **BG[1:0]**[2] **= 3, BA[1:0] = 3** instead | | | | | | | | | | | | | | | | |
| | | 12 | 48-51 | repeat Sub-Loop 0, use **BG[1:0]**[2] **= 2, BA[1:0] = 1** instead | | | | | | | | | | | | | | | | |
| | | 13 | 52-55 | repeat Sub-Loop 1, use **BG[1:0]**[2] **= 3, BA[1:0] = 2** instead | | | | | | | | | | | | | | | | |
| | | 14 | 56-59 | repeat Sub-Loop 0, use **BG[1:0]**[2] **= 2, BA[1:0] = 3** instead | | | | | | | | | | | | | | | | |
| | | 15 | 60-63 | repeat Sub-Loop 1, use **BG[1:0]**[2] **= 3, BA[1:0] = 0** instead | | | | | | | | | | | | | | | | |

**NOTE :**
1. DQS_t, DQS_c are used according to RD Commands, otherwise VDDQ.
2. BG1 is don't care for x16 device
3. C[2:0] are used only for 3DS device
4. Burst Sequence driven on each DQ signal by Read Command.

**[ Table 43 ] IDD4W, IDD4WA, IDD4WB and IDD4W_par Measurement-Loop Pattern[1]**

| CK_t, CK_c | CKE | Sub-Loop | Cycle Number | Command | CS_n | ACT_n | RAS_n | CAS_n/A15 | WE_n/A14 | ODT | C[2:0][3] | BG[1:0][2] | BA[1:0] | A12/BC_n | A[13,11] | A[10]/AP | A[9:7] | A[6:3] | A[2:0] | Data[4] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| toggling | Static High | 0 | 0 | **WR** | 0 | 1 | 1 | 0 | 0 | 1 | 0 | **0** | **0** | 0 | 0 | 0 | **0** | **0** | 0 | **D0=00, D1=FF D2=FF, D3=00 D4=FF, D5=00 D6=00, D7=FF** |
| | | | 1 | D | 1 | 0 | 0 | 0 | 0 | 1 | 0 | **0** | **0** | 0 | 0 | 0 | **0** | **0** | 0 | - |
| | | | 2,3 | D#, D# | 1 | 1 | 1 | 1 | 1 | 1 | 0 | **3**[2] | **3** | 0 | 0 | 0 | **7** | **F** | 0 | - |
| | | 1 | 4 | **WR** | 0 | 1 | 1 | 0 | 0 | 1 | 0 | **1** | **1** | 0 | 0 | 0 | **7** | **F** | 0 | **D0=FF, D1=00 D2=00, D3=FF D4=00, D5=FF D6=FF, D7=00** |
| | | | 5 | D | 1 | 0 | 0 | 0 | 0 | 1 | 0 | **0** | **0** | 0 | 0 | 0 | **0** | **0** | 0 | - |
| | | | 6,7 | D#, D# | 1 | 1 | 1 | 1 | 1 | 1 | 0 | **3**[2] | **3** | 0 | 0 | 0 | **7** | **F** | 0 | - |
| | | 2 | 8-11 | repeat Sub-Loop 0, use **BG[1:0][2] = 0, BA[1:0] = 2** instead | | | | | | | | | | | | | | | | |
| | | 3 | 12-15 | repeat Sub-Loop 1, use **BG[1:0][2] = 1, BA[1:0] = 3** instead | | | | | | | | | | | | | | | | |
| | | 4 | 16-19 | repeat Sub-Loop 0, use **BG[1:0][2] = 0, BA[1:0] = 1** instead | | | | | | | | | | | | | | | | |
| | | 5 | 20-23 | repeat Sub-Loop 1, use **BG[1:0][2] = 1, BA[1:0] = 2** instead | | | | | | | | | | | | | | | | |
| | | 6 | 24-27 | repeat Sub-Loop 0, use **BG[1:0][2] = 0, BA[1:0] = 3** instead | | | | | | | | | | | | | | | | |
| | | 7 | 28-31 | repeat Sub-Loop 1, use **BG[1:0][2] = 1, BA[1:0] = 0** instead | | | | | | | | | | | | | | | | |
| | | 8 | 32-35 | repeat Sub-Loop 0, use **BG[1:0][2] = 2, BA[1:0] = 0** instead | | | | | | | | | | | | | | | | For x4 and x8 only |
| | | 9 | 36-39 | repeat Sub-Loop 1, use **BG[1:0][2] = 3, BA[1:0] = 1** instead | | | | | | | | | | | | | | | | |
| | | 10 | 40-43 | repeat Sub-Loop 0, use **BG[1:0][2] = 2, BA[1:0] = 2** instead | | | | | | | | | | | | | | | | |
| | | 11 | 44-47 | repeat Sub-Loop 1, use **BG[1:0][2] = 3, BA[1:0] = 3** instead | | | | | | | | | | | | | | | | |
| | | 12 | 48-51 | repeat Sub-Loop 0, use **BG[1:0][2] = 2, BA[1:0] = 1** instead | | | | | | | | | | | | | | | | |
| | | 13 | 52-55 | repeat Sub-Loop 1, use **BG[1:0][2] = 3, BA[1:0] = 2** instead | | | | | | | | | | | | | | | | |
| | | 14 | 56-59 | repeat Sub-Loop 0, use **BG[1:0][2] = 2, BA[1:0] = 3** instead | | | | | | | | | | | | | | | | |
| | | 15 | 60-63 | repeat Sub-Loop 1, use **BG[1:0][2] = 3, BA[1:0] = 0** instead | | | | | | | | | | | | | | | | |

**NOTE :**
1. DQS_t, DQS_c are used according to WR Commands, otherwise VDDQ.
2. BG1 is don't care for x16 device
3. C[2:0] are used only for 3DS device
4. Burst Sequence driven on each DQ signal by Write Command.

**[ Table 44 ] IDD4WC Measurement-Loop Pattern[1]**

| CK_t, CK_c | CKE | Sub-Loop | Cycle Number | Command | CS_n | ACT_n | RAS_n | CAS_n/A15 | WE_n/A14 | ODT | C[2:0][3] | BG[1:0][2] | BA[1:0] | A12/BC_n | A[13,11] | A[10]/AP | A[9:7] | A[6:3] | A[2:0] | Data[4] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| toggling | Static High | 0 | 0 | **WR** | 0 | 1 | 1 | 0 | 0 | 1 | 0 | **0** | **0** | 0 | 0 | 0 | **0** | **0** | 0 | **D0=00, D1=FF D2=FF, D3=00 D4=FF, D5=00 D6=00, D7=FF D8=CRC** |
| | | | 1,2 | D, D | 1 | 0 | 0 | 0 | 0 | 1 | 0 | **0** | **0** | 0 | 0 | 0 | **0** | **0** | 0 | - |
| | | | 3,4 | D#, D# | 1 | 1 | 1 | 1 | 1 | 1 | 0 | **3**[2] | **3** | 0 | 0 | 0 | **7** | **F** | 0 | - |
| | | | 5 | **WR** | 0 | 1 | 1 | 0 | 0 | 1 | 0 | **1** | **1** | 0 | 0 | 0 | **7** | **F** | 0 | **D0=FF, D1=00 D2=00, D3=FF D4=00, D5=FF D6=FF, D7=00 D8=CRC** |
| | | | 6,7 | D, D | 1 | 0 | 0 | 0 | 0 | 1 | 0 | **0** | **0** | 0 | 0 | 0 | **0** | **0** | 0 | - |
| | | | 8,9 | D#, D# | 1 | 1 | 1 | 1 | 1 | 1 | 0 | **3**[2] | **3** | 0 | 0 | 0 | **7** | **F** | 0 | - |
| | | 2 | 10-14 | repeat Sub-Loop 0, use **BG[1:0][2] = 0, BA[1:0] = 2** instead | | | | | | | | | | | | | | | | |
| | | 3 | 15-19 | repeat Sub-Loop 1, use **BG[1:0][2] = 1, BA[1:0] = 3** instead | | | | | | | | | | | | | | | | |
| | | 4 | 20-24 | repeat Sub-Loop 0, use **BG[1:0][2] = 0, BA[1:0] = 1** instead | | | | | | | | | | | | | | | | |
| | | 5 | 25-29 | repeat Sub-Loop 1, use **BG[1:0][2] = 1, BA[1:0] = 2** instead | | | | | | | | | | | | | | | | |
| | | 6 | 30-34 | repeat Sub-Loop 0, use **BG[1:0][2] = 0, BA[1:0] = 3** instead | | | | | | | | | | | | | | | | |
| | | 7 | 35-39 | repeat Sub-Loop 1, use **BG[1:0][2] = 1, BA[1:0] = 0** instead | | | | | | | | | | | | | | | | |
| | | 8 | 40-44 | repeat Sub-Loop 0, use **BG[1:0][2] = 2, BA[1:0] = 0** instead | | | | | | | | | | | | | | | | For x4 and x8 only |
| | | 9 | 45-49 | repeat Sub-Loop 1, use **BG[1:0][2] = 3, BA[1:0] = 1** instead | | | | | | | | | | | | | | | | |
| | | 10 | 50-54 | repeat Sub-Loop 0, use **BG[1:0][2] = 2, BA[1:0] = 2** instead | | | | | | | | | | | | | | | | |
| | | 11 | 55-59 | repeat Sub-Loop 1, use **BG[1:0][2] = 3, BA[1:0] = 3** instead | | | | | | | | | | | | | | | | |
| | | 12 | 60-64 | repeat Sub-Loop 0, use **BG[1:0][2] = 2, BA[1:0] = 1** instead | | | | | | | | | | | | | | | | |
| | | 13 | 65-69 | repeat Sub-Loop 1, use **BG[1:0][2] = 3, BA[1:0] = 2** instead | | | | | | | | | | | | | | | | |
| | | 14 | 70-74 | repeat Sub-Loop 0, use **BG[1:0][2] = 2, BA[1:0] = 3** instead | | | | | | | | | | | | | | | | |
| | | 15 | 75-79 | repeat Sub-Loop 1, use **BG[1:0][2] = 3, BA[1:0] = 0** instead | | | | | | | | | | | | | | | | |

**NOTE :**
1. DQS_t, DQS_c are VDDQ.
2. BG1 is don't care for x16 device.
3. C[2:0] are used only for 3DS device.
4. Burst Sequence driven on each DQ signal by Write Command.

**[ Table 45 ] IDD5B Measurement-Loop Pattern[1]**

| CK_t, CK_c | CKE | Sub-Loop | Cycle Number | Command | CS_n | ACT_n | RAS_n | CAS_n/A15 | WE_n/A14 | ODT | C[2:0][3] | BG[1:0][2] | BA[1:0] | A12/BC_n | A[13,11] | A[10]/AP | A[9:7] | A[6:3] | A[2:0] | Data[4] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| toggling | Static High | 0 | 0 | **REF** | 1 | 0 | 0 | 0 | 0 | 0 | 0 | **0** | **0** | 0 | 0 | 0 | **0** | **0** | 0 | - |
| | | 1 | 1 | D | 1 | 0 | 0 | 0 | 0 | 0 | 0 | **0** | **0** | 0 | 0 | 0 | **0** | **0** | 0 | - |
| | | | 2 | D | 1 | 0 | 0 | 0 | 0 | 0 | 0 | **0** | **0** | 0 | 0 | 0 | **0** | **0** | 0 | - |
| | | | 3 | D#, D# | 1 | 1 | 1 | 1 | 1 | 0 | 0 | **3**[2] | **3** | 0 | 0 | 0 | **7** | **F** | 0 | - |
| | | | 4 | D#, D# | 1 | 1 | 1 | 1 | 1 | 0 | 0 | **3**[2] | **3** | 0 | 0 | 0 | **7** | **F** | 0 | - |
| | | | 4-7 | repeat pattern 1...4, use **BG[1:0]**[2] **= 1, BA[1:0] = 1** instead | | | | | | | | | | | | | | | | |
| | | | 8-11 | repeat pattern 1...4, use **BG[1:0]**[2] **= 0, BA[1:0] = 2** instead | | | | | | | | | | | | | | | | |
| | | | 12-15 | repeat pattern 1...4, use **BG[1:0]**[2] **= 1, BA[1:0] = 3** instead | | | | | | | | | | | | | | | | |
| | | | 16-19 | repeat pattern 1...4, use **BG[1:0]**[2] **= 0, BA[1:0] = 1** instead | | | | | | | | | | | | | | | | |
| | | | 20-23 | repeat pattern 1...4, use **BG[1:0]**[2] **= 1, BA[1:0] = 2** instead | | | | | | | | | | | | | | | | |
| | | | 24-27 | repeat pattern 1...4, use **BG[1:0]**[2] **= 0, BA[1:0] = 3** instead | | | | | | | | | | | | | | | | |
| | | | 28-31 | repeat pattern 1...4, use **BG[1:0]**[2] **= 1, BA[1:0] = 0** instead | | | | | | | | | | | | | | | | |
| | | | 32-35 | repeat pattern 1...4, use **BG[1:0]**[2] **= 2, BA[1:0] = 0** instead | | | | | | | | | | | | | | | | For x4 and x8 only |
| | | | 36-39 | repeat pattern 1...4, use **BG[1:0]**[2] **= 3, BA[1:0] = 1** instead | | | | | | | | | | | | | | | | |
| | | | 40-43 | repeat pattern 1...4, use **BG[1:0]**[2] **= 2, BA[1:0] = 2** instead | | | | | | | | | | | | | | | | |
| | | | 44-47 | repeat pattern 1...4, use **BG[1:0]**[2] **= 3, BA[1:0] = 3** instead | | | | | | | | | | | | | | | | |
| | | | 48-51 | repeat pattern 1...4, use **BG[1:0]**[2] **= 2, BA[1:0] = 1** instead | | | | | | | | | | | | | | | | |
| | | | 52-55 | repeat pattern 1...4, use **BG[1:0]**[2] **= 3, BA[1:0] = 2** instead | | | | | | | | | | | | | | | | |
| | | | 56-59 | repeat pattern 1...4, use **BG[1:0]**[2] **= 2, BA[1:0] = 3** instead | | | | | | | | | | | | | | | | |
| | | | 60-63 | repeat pattern 1...4, use **BG[1:0]**[2] **= 3, BA[1:0] = 0** instead | | | | | | | | | | | | | | | | |
| | | 2 | 64 ... nRFC - 1 | repeat Sub-Loop 1, Truncate, if necessary | | | | | | | | | | | | | | | | |

**NOTE :**
1. DQS_t, DQS_c are VDDQ.
2. BG1 is don't care for x16 device.
3. C[2:0] are used only for 3DS device.
4. DQ signals are VDDQ.

**[ Table 46 ] IDD7 Measurement-Loop Pattern[1]**

| CK_t, CK_c | CKE | Sub-Loop | Cycle Number | Command | CS_n | ACT_n | RAS_n | CAS_n/A15 | WE_n/A14 | ODT | C[2:0][3] | BG[1:0][2] | BA[1:0] | A12/BC_n | A[13,11] | A[10]/AP | A[9:7] | A[6:3] | A[2:0] | Data[4] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| toggling | Static High | 0 | 0 | **ACT** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | **0** | **0** | 0 | 0 | 0 | **0** | **0** | 0 | **-** |
| | | | 1 | **RDA** | 0 | 1 | 1 | 0 | 1 | 0 | | **0** | **0** | 0 | 0 | 1 | **0** | **0** | 0 | **D0=00, D1=FF D2=FF, D3=00 D4=FF, D5=00 D6=00, D7=FF** |
| | | | 2 | D | 1 | 0 | 0 | 0 | 0 | 0 | 0 | **0** | **0** | 0 | 0 | 0 | **0** | **0** | 0 | - |
| | | | 3 | D# | 1 | 1 | 1 | 1 | 1 | 0 | 0 | **3**[2] | **3** | 0 | 0 | 0 | **7** | **F** | 0 | - |
| | | | ... | repeat pattern 2...3 until nRRD - 1, if nRRD > 4. Truncate if necessary | | | | | | | | | | | | | | | | |
| | | 1 | nRRD | **ACT** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | **1** | **1** | 0 | 0 | 0 | **0** | **0** | 0 | **-** |
| | | | nRRD + 1 | **RDA** | 0 | 1 | 1 | 0 | 1 | 0 | | **1** | **1** | 0 | 0 | 1 | **0** | **0** | 0 | **D0=FF, D1=00 D2=00, D3=FF D4=00, D5=FF D6=FF, D7=00** |
| | | | ... | repeat pattern 2 ... 3 until 2*nRRD - 1, if nRRD > 4. Truncate if necessary | | | | | | | | | | | | | | | | |
| | | 2 | 2*nRRD | repeat Sub-Loop 0, use **BG[1:0][2] = 0, BA[1:0] = 2** instead | | | | | | | | | | | | | | | | |
| | | 3 | 3*nRRD | repeat Sub-Loop 1, use **BG[1:0][2] = 1, BA[1:0] = 3** instead | | | | | | | | | | | | | | | | |
| | | 4 | 4*nRRD | repeat pattern 2 ... 3 until nFAW - 1, if nFAW > 4*nRRD. Truncate if necessary | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | |
| | | 5 | nFAW | repeat Sub-Loop 0, use **BG[1:0][2] = 0, BA[1:0] = 1** instead | | | | | | | | | | | | | | | | |
| | | 6 | nFAW + nRRD | repeat Sub-Loop 1, use **BG[1:0][2] = 1, BA[1:0] = 2** instead | | | | | | | | | | | | | | | | |
| | | 7 | nFAW + 2*nRRD | repeat Sub-Loop 0, use **BG[1:0][2] = 0, BA[1:0] = 3** instead | | | | | | | | | | | | | | | | |
| | | 8 | nFAW + 3*nRRD | repeat Sub-Loop 1, use **BG[1:0][2] = 1, BA[1:0] = 0** instead | | | | | | | | | | | | | | | | |
| | | 9 | nFAW + 4*nRRD | repeat Sub-Loop 4 | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | |
| | | 10 | 2*nFAW | repeat Sub-Loop 0, use **BG[1:0][2] = 2, BA[1:0] = 0** instead | | | | | | | | | | | | | | | | For x4 and x8 only |
| | | 11 | 2*nFAW + nRRD | repeat Sub-Loop 1, use **BG[1:0][2] = 3, BA[1:0] = 1** instead | | | | | | | | | | | | | | | | |
| | | 12 | 2*nFAW + 2*nRRD | repeat Sub-Loop 0, use **BG[1:0][2] = 2, BA[1:0] = 2** instead | | | | | | | | | | | | | | | | |
| | | 13 | 2*nFAW + 3*nRRD | repeat Sub-Loop 1, use **BG[1:0][2] = 3, BA[1:0] = 3** instead | | | | | | | | | | | | | | | | |
| | | 14 | 2*nFAW + 4*nRRD | repeat Sub-Loop 4 | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | |
| | | 15 | 3*nFAW | repeat Sub-Loop 0, use **BG[1:0][2] = 2, BA[1:0] = 1** instead | | | | | | | | | | | | | | | | |
| | | 16 | 3*nFAW + nRRD | repeat Sub-Loop 1, use **BG[1:0][2] = 3, BA[1:0] = 2** instead | | | | | | | | | | | | | | | | |
| | | 17 | 3*nFAW + 2*nRRD | repeat Sub-Loop 0, use **BG[1:0][2] = 2, BA[1:0] = 3** instead | | | | | | | | | | | | | | | | |
| | | 18 | 3*nFAW + 3*nRRD | repeat Sub-Loop 1, use **BG[1:0][2] = 3, BA[1:0] = 0** instead | | | | | | | | | | | | | | | | |
| | | 19 | 3*nFAW + 4*nRRD | repeat Sub-Loop 4 | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | |
| | | 20 | 4*nFAW | repeat pattern 2 ... 3 until nRC - 1, if nRC > 4*nFAW. Truncate if necessary | | | | | | | | | | | | | | | | |

**NOTE :**
1. DQS_t, DQS_c are VDDQ.
2. BG1 is don't care for x16 device.
3. C[2:0] are used only for 3DS device.
4. Burst Sequence driven on each DQ signal by Read Command. Outside burst operation, DQ signals are VDDQ.

# 12.8Gb DDR4 SDRAM C-die IDD Specification Table

IDD and IPP values are for typical operating range of voltage and temperature unless otherwise noted.

**[ Table 47 ] $I_{DD}$ and $I_{DDQ}$ Specification**

| Symbol | 2Gx4 (K4A8G045WC) | | | 1Gx8 (K4A8G085WC) | | | Unit | NOTE |
|---|---|---|---|---|---|---|---|---|
| | DDR4-2133 | DDR4-2400 | DDR4-2666 | DDR4-2133 | DDR4-2400 | DDR4-2666 | | |
| | 15-15-15 | 17-17-17 | 19-19-19 | 15-15-15 | 17-17-17 | 19-19-19 | | |
| | VDD 1.2V | VDD 1.2V | VDD 1.2V | VDD 1.2V | VDD 1.2V | VDD 1.2V | | |
| | IDD Max. | IDD Max. | IDD Max. | IDD Max. | IDD Max. | IDD Max. | | |
| $I_{DD0}$ | 25 | 25 | 26 | 27 | 27 | 28 | mA | |
| $I_{DD0A}$ | 26 | 28 | 29 | 29 | 29 | 31 | mA | |
| $I_{DD1}$ | 29 | 29 | 29 | 32 | 32 | 32 | mA | |
| $I_{DD1A}$ | 32 | 32 | 35 | 33 | 34 | 38 | mA | |
| $I_{DD2N}$ | 17 | 18 | 18 | 17 | 18 | 18 | mA | |
| $I_{DD2NA}$ | 20 | 21 | 21 | 17 | 18 | 21 | mA | |
| $I_{DD2NT}$ | 20 | 21 | 21 | 17 | 18 | 21 | mA | |
| $I_{DD2NL}$ | 10 | 12 | 12 | 13 | 14 | 14 | mA | |
| $I_{DD2NG}$ | 17 | 18 | 18 | 16 | 17 | 18 | mA | |
| $I_{DD2ND}$ | 15 | 16 | 16 | 16 | 17 | 17 | mA | |
| $I_{DD2N_par}$ | 18 | 19 | 19 | 18 | 19 | 19 | mA | |
| $I_{DD2P}$ | 11 | 11 | 11 | 11 | 11 | 11 | mA | |
| $I_{DD2Q}$ | 16 | 17 | 17 | 16 | 17 | 17 | mA | |
| $I_{DD3N}$ | 25 | 25 | 25 | 27 | 27 | 27 | mA | |
| $I_{DD3NA}$ | 27 | 27 | 27 | 28 | 28 | 29 | mA | |
| $I_{DD3P}$ | 19 | 19 | 19 | 19 | 19 | 19 | mA | |
| $I_{DD4R}$ | 62 | 67 | 83 | 76 | 82 | 99 | mA | |
| $I_{DD4RA}$ | 66 | 71 | 89 | 79 | 86 | 105 | mA | |
| $I_{DD4RB}$ | 62 | 67 | 83 | 79 | 85 | 100 | mA | |
| $I_{DD4W}$ | 65 | 71 | 82 | 74 | 80 | 92 | mA | |
| $I_{DD4WA}$ | 69 | 76 | 87 | 78 | 85 | 97 | mA | |
| $I_{DD4WB}$ | 65 | 72 | 83 | 74 | 80 | 93 | mA | |
| $I_{DD4WC}$ | 57 | 67 | 76 | 67 | 71 | 85 | mA | |
| $I_{DD4W_par}$ | 73 | 81 | 94 | 81 | 89 | 103 | mA | |
| $I_{DD5B}$ | 218 | 218 | 218 | 185 | 185 | 185 | mA | |
| $I_{DD5F2}$ | 154 | 154 | 154 | 130 | 130 | 130 | mA | |
| $I_{DD5F4}$ | 132 | 132 | 132 | 108 | 108 | 108 | mA | |
| $I_{DD6N}$ | 21 | 21 | 21 | 21 | 21 | 21 | mA | |
| $I_{DD6E}$ | 32 | 32 | 32 | 34 | 34 | 34 | mA | |
| $I_{DD6R}$ | 14 | 14 | 14 | 15 | 15 | 15 | mA | |
| $I_{DD6A}$ | 20 | 20 | 20 | 21 | 21 | 21 | mA | |
| $I_{DD7}$ | 132 | 147 | 169 | 132 | 135 | 147 | mA | |
| $I_{DD8}$ | 10 | 10 | 10 | 9 | 9 | 10 | mA | |

**[ Table 48 ] $I_{PP}$ Specification**

| Symbol | 2Gx4 (K4A8G0485WC) | | | 1Gx8 (K4A8G085WC) | | | Unit | NOTE |
|---|---|---|---|---|---|---|---|---|
| | DDR4-2133 | DDR4-2400 | DDR4-2666 | DDR4-2133 | DDR4-2400 | DDR4-2666 | | |
| | 15-15-15 | 17-17-17 | 19-19-19 | 15-15-15 | 17-17-17 | 19-19-19 | | |
| | VPP 2.5V | VPP 2.5V | VPP 2.5V | VPP 2.5V | VPP 2.5V | VPP 2.5V | | |
| | IPP Max. | IPP Max. | IPP Max. | IPP Max. | IPP Max. | IPP Max. | | |
| $I_{PP0}$ | 4 | 4 | 4 | 4 | 4 | 4 | mA | |
| $I_{PP1}$ | 4 | 4 | 4 | 4 | 4 | 4 | mA | |
| $I_{PP2N}$ | 3 | 3 | 3 | 3 | 3 | 3 | mA | |
| $I_{PP2P}$ | 3 | 3 | 3 | 3 | 3 | 3 | mA | |
| $I_{PP3N}$ | 4 | 4 | 4 | 3 | 3 | 4 | mA | |
| $I_{PP3P}$ | 4 | 4 | 4 | 3 | 3 | 4 | mA | |
| $I_{PP4R}$ | 4 | 4 | 4 | 3 | 3 | 4 | mA | |
| $I_{PP4W}$ | 3 | 3 | 3 | 3 | 3 | 3 | mA | |
| $I_{PP5B}$ | 21 | 21 | 21 | 18 | 18 | 18 | mA | |
| $I_{PP5F2}$ | 15 | 15 | 15 | 15 | 15 | 15 | mA | |
| $I_{PP5F4}$ | 14 | 14 | 14 | 14 | 14 | 14 | mA | |
| $I_{PP6N}$ | 4 | 4 | 4 | 4 | 4 | 4 | mA | |
| $I_{PP6E}$ | 5 | 5 | 4 | 5 | 5 | 5 | mA | |
| $I_{PP7}$ | 10 | 11 | 12 | 10 | 10 | 11 | mA | |
| $I_{PP8}$ | 3 | 3 | 3 | 3 | 3 | 3 | mA | |

**[ Table 49 ] $I_{DD6}$ Specification**

| Symbol | Temperature Range | Value | | | Value | | | Unit | NOTE |
|---|---|---|---|---|---|---|---|---|---|
| | | 2Gx4 (K4A8G045WC) | | | 1Gx8 (K4A8G085WC) | | | | |
| | | DDR4-2133 | DDR4-2400 | DDR4-2666 | DDR4-2133 | DDR4-2400 | DDR4-2666 | | |
| | | 15-15-15 | 17-17-17 | 19-19-19 | 15-15-15 | 17-17-17 | 19-19-19 | | |
| | | 1.2V | | | 1.2V | | | | |
| $I_{DD6N}$ | 0 - 85 °C | 21 | 21 | 21 | 21 | 21 | 21 | mA | 1,2 |
| $I_{DD6E}$ | 0 - 95 °C | 32 | 32 | 32 | 34 | 34 | 34 | mA | 2,3 |

**NOTE :**
1. Applicable for MR2 settings A6=0 and A7=0.
2. Include a max value for $I_{DD6}$.
3. Applicable for MR2 settings A6=0 and A7=1. $I_{DD6E}$ is only specified for devices which support the Extended Temperature Range feature.

# 13. Input/Output Capacitance

**[ Table 50 ] Silicon Pad I/O Capacitance**

| Symbol | Parameter | DDR4-1600/1866/2133 | | DDR4-2400/2666 | | Unit | NOTE |
|---|---|---|---|---|---|---|---|
| | | min | max | min | max | | |
| $C_{IO}$ | Input/output capacitance | 0.55 | 1.4 | 0.55 | 1.15 | pF | 1,2,3 |
| $C_{DIO}$ | Input/output capacitance delta | -0.1 | 0.1 | -0.1 | 0.1 | pF | 1,2,3,11 |
| $C_{DDQS}$ | Input/output capacitance delta DQS_t and DQS_c | - | 0.05 | - | 0.05 | pF | 1,2,3,5 |
| $C_{CK}$ | Input capacitance, CK_t and CK_c | 0.2 | 0.8 | 0.2 | 0.7 | pF | 1,3 |
| $C_{DCK}$ | Input capacitance delta CK_t and CK_c | - | 0.05 | - | 0.05 | pF | 1,3,4 |
| $C_{I}$ | Input capacitance(CTRL, ADD, CMD pins only) | 0.2 | 0.8 | 0.2 | 0.7 | pF | 1,3,6 |
| $C_{DI_CTRL}$ | Input capacitance delta(All CTRL pins only) | -0.1 | 0.1 | -0.1 | 0.1 | pF | 1,3,7,8 |
| $C_{DI_ADD_CMD}$ | Input capacitance delta(All ADD/CMD pins only) | -0.1 | 0.1 | -0.1 | 0.1 | pF | 1,2,9,10 |
| $C_{ALERT}$ | Input/output capacitance of ALERT | 0.5 | 1.5 | 0.5 | 1.5 | pF | 1,3 |
| $C_{ZQ}$ | Input/output capacitance of ZQ | - | 2.3 | - | 2.3 | pF | 1,3,12 |
| $C_{TEN}$ | Input capacitance of TEN | 0.2 | 2.3 | 0.2 | 2.3 | pF | 1,3,13 |

**NOTE:**

1. This parameter is not subject to production test. It is verified by design and characterization. The silicon only capacitance is validated by de-embedding the package L & C parasitic. The capacitance is measured with VDD, VDDQ, VSS, VSSQ applied with all other signal pins floating. Measurement procedure tbd.
2. DQ, DM_n, DQS_T, DQS_C, TDQS_T, TDQS_C. Although the DM, TDQS_T and TDQS_C pins have different functions, the loading matches DQ and DQS
3. This parameter applies to monolithic devices only; stacked/dual-die devices are not covered here
4. Absolute value CK_T-CK_C
5. Absolute value of CIO(DQS_T)-CIO(DQS_C)
6. CI applies to ODT, CS_n, CKE, A0-A15, BA0-BA1, BG0-BG1, RAS_n, CAS_n/A15, WE_n/A14, ACT_n and PAR.
7. CDI CTRL applies to ODT, CS_n and CKE
8. CDI_CTRL = CI(CTRL)-0.5*(CI(CLK_T)+CI(CLK_C))
9. CDI_ADD_ CMD applies to, A0-A15, BA0-BA1, BG0-BG1,RAS_n, CAS_n/A15, WE_n/A14, ACT_n and PAR.
10. CDI_ADD_CMD = CI(ADD_CMD)-0.5*(CI(CLK_T)+CI(CLK_C))
11. CDIO = CIO(DQ,DM)-0.5*(CIO(DQS_T)+CIO(DQS_C))
12. Maximum external load capacitance on ZQ pin: tbd pF.
13. TEN pin may be DRAM internally pulled low through a weak pull-down resistor to VSS. In this case $C_{TEN}$ might not be valid and system shall verify TEN signal with Vendor specific information.

**[ Table 51 ] DRAM Package Electrical Specifications (x4/x8)**

| Symbol | Parameter | DDR4-1600/1866/2133/2400 | | DDR4-2666 | | Unit | NOTE |
|---|---|---|---|---|---|---|---|
| | | min | max | min | max | | |
| $Z_{IO}$ | Input/output Zpkg | 45 | 85 | 45 | 85 | Ω | 1,2,4,5,10,11 |
| $T_{dIO}$ | Input/output Pkg Delay | 14 | 42 | 14 | 42 | ps | 1,3,4,5,11 |
| $L_{io}$ | Input/Output Lpkg | - | 3.3 | - | 3.3 | nH | 11,12 |
| $C_{io}$ | Input/Output Cpkg | - | 0.78 | - | 0.78 | pF | 11,13 |
| $Z_{IO\ DQS}$ | DQS_t, DQS_c Zpkg | 45 | 85 | 45 | 85 | Ω | 1,2,5,10,11 |
| $Td_{IO\ DQS}$ | DQS_t, DQS_c Pkg Delay | 14 | 42 | 14 | 42 | ps | 1,3,5,10,11 |
| $L_{io\ DQS}$ | DQS Lpkg | - | 3.3 | - | 3.3 | nH | 11,12 |
| $C_{io\ DQS}$ | DQS Cpkg | - | 0.78 | - | 0.78 | pF | 11,13 |
| $DZ_{DIO\ DQS}$ | Delta Zpkg DQS_t, DQS_c | - | 10 | - | 10 | Ω | 1,2,5,7,10 |
| $D_{TdDIO\ DQS}$ | Delta Delay DQS_t, DQS_c | - | 5 | - | 5 | ps | 1,3,5,7,10 |
| $Z_{I\ CTRL}$ | Input- CTRL pins Zpkg | 50 | 90 | 50 | 90 | Ω | 1,2,5,9,10,11 |
| $T_{dI_\ CTRL}$ | Input- CTRL pins Pkg Delay | 14 | 42 | 14 | 42 | ps | 1,3,5,9,10,11 |
| $L_{i\ CTRL}$ | Input CTRL Lpkg | - | 3.4 | - | 3.4 | nH | 11,12 |
| $C_{i\ CTRL}$ | Input CTRL Cpkg | - | 0.7 | - | 0.7 | pF | 11,13 |
| $Z_{IADD\ CMD}$ | Input- CMD ADD pins Zpkg | 50 | 90 | 50 | 90 | Ω | 1,2,5,8,10,11 |
| $Td_{IADD_\ CMD}$ | Input- CMD ADD pins Pkg Delay | 14 | 45 | 14 | 45 | ps | 1,3,5,8,10,11 |
| $L_{i\ ADD\ CMD}$ | Input CMD ADD Lpkg | - | 3.6 | - | 3.6 | nH | 11,12 |
| $C_{i\ ADD\ CMD}$ | Input CMD ADD Cpkg | - | 0.74 | - | 0.74 | pF | 11,13 |
| $Z_{CK}$ | CLK_t & CLK_c Zpkg | 50 | 90 | 50 | 90 | Ω | 1,2,5,10,11 |
| $Td_{CK}$ | CLK_t & CLK_c Pkg Delay | 14 | 42 | 14 | 42 | ps | 1,3,5,10,11 |
| $L_{i\ CLK}$ | Input CLK Lpkg | - | 3.4 | - | 3.4 | nH | 11,12 |
| $C_{i\ CLK}$ | Input CLK Cpkg | - | 0.7 | - | 0.7 | pF | 11,13 |
| $DZ_{DCK}$ | Delta Zpkg CLK_t & CLK_c | - | 10 | - | 10 | Ω | 1,2,5,6,10 |
| $D_{TdCK}$ | Delta Delay CLK_t & CLK_c | - | 5 | - | 5 | ps | 1,3,5,6,10 |
| $Z_{OZQ}$ | ZQ Zpkg | - | 100 | - | 100 | Ω | 1,2,5,10,11 |
| $Td_{O\ ZQ}$ | ZQ Delay | 20 | 90 | 20 | 90 | ps | 1,3,5,10,11 |
| $Z_{O\ ALERT}$ | ALERT Zpkg | 40 | 100 | 40 | 100 | Ω | 1,2,5,10,11 |
| $Td_{O\ ALERT}$ | ALERT Delay | 20 | 55 | 20 | 55 | ps | 1,3,5,10,11 |

**NOTE :**

1. This parameter is not subject to production test. It is verified by design and characterization. The package parasitic( L & C) are validated using package only samples. The capacitance is measured with VDD, VDDQ, VSS, VSSQ shorted with all other signal pins floating. The inductance is measured with VDD, VDDQ, VSS and VSSQ shorted and all other signal pins shorted at the die side(not pin). Measurement procedure tbd
2. Package only impedance (Zpkg) is calculated based on the Lpkg and Cpkg total for a given pin where:

$$Zpkg(\text{total per pin}) = \sqrt{Lpkg/Cpkg}$$

3. Package only delay(Tpkg) is calculated based on Lpkg and Cpkg total for a given pin where:

$$Tdpkg(\text{total per pin}) = \sqrt{Lpkg * Cpkg}$$

4. Z & Td IO applies to DQ, DM, TDQS_T and TDQS_C
5. This parameter applies to monolithic devices only; stacked/dual-die devices are not covered here
6. Absolute value of ZCK_t-ZCK_c for impedance(Z) or absolute value of TdCK_t-TdCK_c for delay(Td).
7. Absolute value of ZIO(DQS_t)-ZIO(DQS_c) for impedance(Z) or absolute value of TdIO(DQS_t)-TdIO(DQS_c) for delay(Td)
8. ZI & Td ADD CMD applies to A0-A13,A17, ACT_n, BA0-BA1, BG0-BG1, RAS_n/16, CAS_n/A15, WE_n/A14 and PAR.
9. ZI & Td CTRL applies to ODT, CS_n and CKE
10. This table applies to monolithic X4 and X8 devices.
11. Package implementations shall meet spec if the Zpkg and Pkg Delay fall within the ranges shown, and the maximum Lpkg and Cpkg do not exceed the maximum values shown.
12. It is assumed that Lpkg can be approximated as Lpkg = Zo*Td.
13. It is assumed that Cpkg can be approximated as Cpkg = Td/Zo.

# 14. Electrical Characteristics & AC Timing

## 14.1 Reference Load for AC Timing and Output Slew Rate

Figure 23 represents the effective reference load of 50 ohms used in defining the relevant AC timing parameters of the device as well as output slew rate measurements.

Ron nominal of DQ, DQS_t and DQS_c drivers uses 34 ohms to specify the relevant AC timing paraeter values of the device.

The maximum DC High level of Output signal = 1.0 * VDDQ,

The minimum DC Low level of Output signal = {34 /(34 + 50)} *VDDQ = 0.4* VDDQ

The nominal reference level of an Output signal can be approximated by the following:

The center of maximum DC High and minimum DC Low = {(1 + 0.4) / 2} * VDDQ = 0.7 * VDDQ

The actual reference level of Output signal might vary with driver Ron and reference load tolerances. Thus, the actual reference level or midpoint of an output signal is at the widest part of the output signal's eye. Prior to measuring AC parameters, the reference level of the verification tool should be set to an appropriate level.

It is not intended as a precise representation of any particular system environment or a depiction of the actual load presented by a production tester. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers correlate to their production test conditions, generally one or more coaxial transmission lines terminated at the tester electronics.

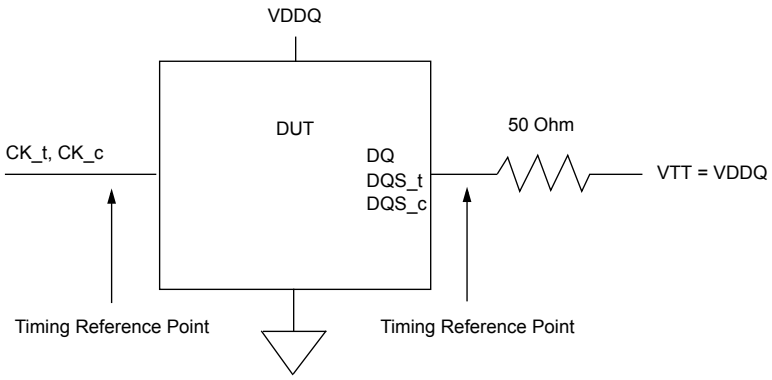



**Figure 23. Reference Load for AC Timing and Output Slew Rate**

## 14.2 tREFI

Average periodic Refresh interval (tREFI) of DDR4 SDRAM is defined as shown in the table.

**[ Table 52 ] tREFI by Device Density**

| Parameter | Symbol | | 2Gb | 4Gb | 8Gb | 16Gb | Units |
|---|---|---|---|---|---|---|---|
| Average periodic refresh interval | tREFI | 0°C ≤ TCASE ≤ 85°C | 7.8 | 7.8 | 7.8 | 7.8 | µs |
| | | 85°C < TCASE ≤ 95°C | 3.9 | 3.9 | 3.9 | 3.9 | µs |

## 14.3 Clock Specification

The jitter specified is a random jitter meeting a Gaussian distribution. Input clocks violating the min/max values may result in malfunction of the DDR4 SDRAM device.

### 14.3.1 Definition for tCK(abs)

tCK(abs) is defined as the absolute clock period, as measured from one rising edge to the next consecutive rising edge. tCK(abs) is not subject t o production test.

### 14.3.2 Definition for tCK(avg)

tCK(avg) is calculated as the average clock period across any consecutive 200 cycle window, where each clock period is calculated from rising edge to rising edge.

$$tCK(avg) = \left( \sum_{j=1}^{N} tCK(abs)j \right) / N \qquad N = 200$$

### 14.3.3 Definition for tCH(avg) and tCL(avg)

tCH(avg) is defined as the average high pulse width, as calculated across any consecutive 200 high pulses.

$$tCH(avg) = \left( \sum_{j=1}^{N} tCHj \right) / \{ N \times tCK(avg) \} \qquad N = 200$$

tCL(avg) is defined as the average low pulse width, as calculated across any consecutive 200 low pulses.

$$tCL(avg) = \left( \sum_{j=1}^{N} tCLj \right) / \{ N \times tCK(avg) \} \qquad N = 200$$

### 14.3.4 Definition for tERR(nper)

tERR is defined as the cumulative error across n consecutive cycles of n x tCK(avg). tERR is not subject to production test.

# 14.4 Timing Parameters by Speed Grade

**[ Table 53 ] Timing Parameters by Speed Bin for DDR4-1600 to DDR4-2666**

| Speed | | DDR4-1600 | | DDR4-1866 | | DDR4-2133 | | DDR4-2400 | | DDR4-2666 | | Units | NOTE |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Parameter | Symbol | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | | |
| **Clock Timing** | | | | | | | | | | | | | |
| Minimum Clock Cycle Time (DLL off mode) | tCK (DLL_OFF) | 8 | 20 | 8 | 20 | 8 | 20 | 8 | 20 | 8 | 20 | ns | |
| Average Clock Period | tCK(avg) | 1.25 | <1.5 | 1.071 | <1.25 | 0.937 | <1.071 | 0.833 | <0.937 | 0.750 | <0.833 | ns | 35,36 |
| Average high pulse width | tCH(avg) | 0.48 | 0.52 | 0.48 | 0.52 | 0.48 | 0.52 | 0.48 | 0.52 | 0.48 | 0.52 | tCK(avg) | |
| Average low pulse width | tCL(avg) | 0.48 | 0.52 | 0.48 | 0.52 | 0.48 | 0.52 | 0.48 | 0.52 | 0.48 | 0.52 | tCK(avg) | |
| Absolute Clock Period | tCK(abs) | tCK(avg)min + tJIT(per)min_tot<br>tCK(avg)m ax + tJIT(per)max_tot | | | | | | | | | | tCK(avg) | |
| Absolute clock HIGH pulse width | tCH(abs) | 0.45 | - | 0.45 | - | 0.45 | - | 0.45 | - | 0.45 | - | tCK(avg) | 23 |
| Absolute clock LOW pulse width | tCL(abs) | 0.45 | - | 0.45 | - | 0.45 | - | 0.45 | - | 0.45 | - | tCK(avg) | 24 |
| Clock Period Jitter- total | JIT(per)_tot | -63 | 63 | -54 | 54 | -47 | 47 | -42 | 42 | -38 | 38 | ps | 23 |
| Clock Period Jitter- deterministic | JIT(per)_dj | -31 | 31 | -27 | 27 | -23 | 23 | -21 | 21 | -19 | 19 | ps | 26 |
| Clock Period Jitter during DLL locking period | tJIT(per, lck) | -50 | 50 | -43 | 43 | -38 | 38 | -33 | 33 | -30 | 30 | ps | |
| Cycle to Cycle Period Jitter | tJIT(cc) | - | 125 | - | 107 | - | 94 | - | 83 | - | 75 | ps | |
| Cycle to Cycle Period Jitter during DLL locking period | tJIT(cc, lck) | - | 100 | - | 86 | - | 75 | - | 67 | - | 60 | ps | |
| Duty Cycle Jitter | tJIT(duty) | TBD | TBD | TBD | TBD | TBD | TBD | TBD | TBD | TBD | TBD | ps | |
| Cumulative error across 2 cycles | tERR(2per) | -92 | 92 | -79 | 79 | -69 | 69 | -61 | 61 | -55 | 55 | ps | |
| Cumulative error across 3 cycles | tERR(3per) | -109 | 109 | -94 | 94 | -82 | 82 | -73 | 73 | -66 | 66 | ps | |
| Cumulative error across 4 cycles | tERR(4per) | -121 | 121 | -104 | 104 | -91 | 91 | -81 | 81 | -73 | 73 | ps | |
| Cumulative error across 5 cycles | tERR(5per) | -131 | 131 | -112 | 112 | -98 | 98 | -87 | 87 | -78 | 78 | ps | |
| Cumulative error across 6 cycles | tERR(6per) | -139 | 139 | -119 | 119 | -104 | 104 | -92 | 92 | -83 | 83 | ps | |
| Cumulative error across 7 cycles | tERR(7per) | -145 | 145 | -124 | 124 | -109 | 109 | -97 | 97 | -87 | 87 | ps | |
| Cumulative error across 8 cycles | tERR(8per) | -151 | 151 | -129 | 129 | -113 | 113 | -101 | 101 | -91 | 91 | ps | |
| Cumulative error across 9 cycles | tERR(9per) | -156 | 156 | -134 | 134 | -117 | 117 | -104 | 104 | -94 | 94 | ps | |
| Cumulative error across 10 cycles | tERR(10per) | -160 | 160 | -137 | 137 | -120 | 120 | -107 | 107 | -96 | 96 | ps | |
| Cumulative error across 11 cycles | tERR(11per) | -164 | 164 | -141 | 141 | -123 | 123 | -110 | 110 | -99 | 99 | ps | |
| Cumulative error across 12 cycles | tERR(12per) | -168 | 168 | -144 | 144 | -126 | 126 | -112 | 112 | -101 | 101 | ps | |
| Cumulative error across 13 cycles | tERR(13per) | -172 | 172 | -147 | 147 | -129 | 129 | -114 | 114 | -103 | 103 | ps | |
| Cumulative error across 14 cycles | tERR(14per) | -175 | 175 | -150 | 150 | -131 | 131 | -116 | 116 | -104 | 104 | ps | |
| Cumulative error across 15 cycles | tERR(15per) | -178 | 178 | -152 | 152 | -133 | 133 | -118 | 118 | -106 | 106 | ps | |
| Cumulative error across 16 cycles | tERR(16per) | -180 | 189 | -155 | 155 | -135 | 135 | -120 | 120 | -108 | 108 | ps | |
| Cumulative error across 17 cycles | tERR(17per) | -183 | 183 | -157 | 157 | -137 | 137 | -122 | 122 | -110 | 110 | ps | |
| Cumulative error across 18 cycles | tERR(18per) | -185 | 185 | -159 | 159 | -139 | 139 | -124 | 124 | -112 | 112 | ps | |
| Cumulative error across n = 13, 14 . . . 49, 50 cycles | tERR(nper) | $^{t}$ERR(nper)min = ((1 + 0.68ln(n)) * $^{t}$JIT(per)_total min)<br>$^{t}$ERR(nper)max = ((1 + 0.68ln(n)) * $^{t}$JIT(per)_total max) | | | | | | | | | | ps | |
| Command and Address setup time to CK_t, CK_c referenced to Vih(ac) / Vil(ac) levels | tIS(base) | 115 | - | 100 | - | 80 | - | 62 | - | TBD | - | ps | |
| Command and Address setup time to CK_t, CK_c referenced to Vref levels | tIS(Vref) | 215 | - | 200 | - | 180 | - | 162 | - | TBD | - | ps | |
| Command and Address hold time to CK_t, CK_c referenced to Vih(dc) / Vil(dc) levels | tIH(base) | 140 | - | 125 | - | 105 | - | 87 | - | TBD | - | ps | |
| Command and Address hold time to CK_t, CK_c referenced to Vref levels | tIH(Vref) | 215 | - | 200 | - | 180 | - | 162 | - | TBD | - | ps | |
| Control and Address Input pulse width for each input | tIPW | 600 | - | 525 | - | 460 | - | 410 | - | 385 | - | ps | |
| **Command and Address Timing** | | | | | | | | | | | | | |
| CAS_n to CAS_n command delay for same bank group | tCCD_L | max(5 nCK, 6.250 ns) | - | max(5 nCK, 5.355 ns) | - | max(5 nCK, 5.625 ns) | - | max(5 nCK, 5 ns) | - | max(5 nCK, 5 ns) | - | nCK | 34 |
| CAS_n to CAS_n command delay for different bank group | tCCD_S | 4 | - | 4 | - | 4 | - | 4 | - | 4 | - | nCK | 34 |
| ACTIVATE to ACTIVATE Command delay to different bank group for 2KB page size | tRRD_S(2K) | Max(4nCK,6ns) | - | Max(4nCK,5.3ns) | - | Max(4nCK,5.3ns) | - | Max(4nCK,5.3ns) | - | Max(4nCK,5.3ns) | - | nCK | 34 |
| ACTIVATE to ACTIVATE Command delay to different bank group for 2KB page size | tRRD_S(1K) | Max(4nCK,5ns) | | Max(4nCK,4.2ns) | | Max(4nCK,3.7ns) | | Max(4nCK,3.3ns) | - | Max(4nCK,3ns) | - | nCK | 34 |
| ACTIVATE to ACTIVATE Command delay to different bank group for 1/2KB page size | tRRD_S(1/2K) | Max(4nCK,5ns) | | Max(4nCK,4.2ns) | | Max(4nCK,3.7ns) | | Max(4nCK,3.3ns) | - | Max(4nCK,3ns) | - | nCK | 34 |
| ACTIVATE to ACTIVATE Command delay to same bank group for 2KB page size | tRRD_L(2K) | Max(4nCK,7.5ns) | | Max(4nCK,6.4ns) | | Max(4nCK,6.4ns) | | Max(4nCK,6.4ns) | - | Max(4nCK,6.4ns) | - | nCK | 34 |

| Speed | | DDR4-1600 | | DDR4-1866 | | DDR4-2133 | | DDR4-2400 | | DDR4-2666 | | Units | NOTE |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Parameter | Symbol | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | | |
| ACTIVATE to ACTIVATE Command delay to same bank group for 1KB page size | tRRD_L(1K) | Max(4nCK,6ns) | | Max(4nCK,5.3ns) | | Max(4nCK,5.3ns) | | Max(4nCK,4.9ns) | - | Max(4nCK,4.9ns) | - | nCK | 34 |
| ACTIVATE to ACTIVATE Command delay to same bank group for 1/2KB page size | tRRD_L(1/2K) | Max(4nCK,6ns) | | Max(4nCK,5.3ns) | | Max(4nCK,5.3ns) | | Max(4nCK,4.9ns) | - | Max(4nCK,4.9ns) | - | nCK | 34 |
| Four activate window for 2KB page size | tFAW_2K | Max(28nCK,35ns) | | Max(28nCK,30ns) | | Max(28nCK,30ns) | | Max(28nCK,30ns) | - | Max(28nCK,30ns) | - | ns | 34 |
| Four activate window for 1KB page size | tFAW_1K | Max(20nCK,25ns) | | Max(20nCK,23ns) | | Max(20nCK,21ns) | | Max(20nCK,21ns) | - | Max(20nCK,21ns) | - | ns | 34 |
| Four activate window for 1/2KB page size | tFAW_1/2K | Max(16nCK,20ns) | | Max(16nCK,17ns) | | Max(16nCK,15ns) | | Max(16nCK,13ns) | - | Max(16nCK,12ns) | - | ns | 34 |
| Delay from start of internal write transaction to internal read command for different bank group | tWTR_S | max(2nCK,2.5ns) | - | max(2nCK,2.5ns) | - | max(2nCK,2.5ns) | - | max (2nCK, 2.5ns) | - | max (2nCK, 2.5ns) | - | ns | 1,2,e,34 |
| Delay from start of internal write transaction to internal read command for same bank group | tWTR_L | max(4nCK,7.5ns) | - | max(4nCK,7.5ns) | - | max(4nCK,7.5ns) | - | max (4nCK,7.5ns) | - | max (4nCK,7.5ns) | - | | 1,34 |
| Internal READ Command to PRECHARGE Command delay | tRTP | max(4nCK,7.5ns) | - | max(4nCK,7.5ns) | - | max(4nCK,7.5ns) | - | max (4nCK,7.5ns) | - | max (4nCK,7.5ns) | - | | 34 |
| WRITE recovery time | tWR | 15 | - | 15 | - | 15 | - | 15 | - | 15 | - | ns | 1 |
| Write recovery time when CRC and DM are enabled | tWR_CRC_DM | tWR+max (4nCK,3.75ns) | - | tWR+max (5nCK,3.75ns) | - | tWR+max (5nCK,3.75ns) | - | tWR+max (5nCK,3.75ns) | - | tWR+max (5nCK,3.75ns) | - | ns | 1, 28 |
| delay from start of internal write transaction to internal read command for different bank group with both CRC and DM enabled | tWTR_S_CRC_DM | tWTR_S+ max (4nCK,3.75ns) | - | tWTR_S+ max (5nCK,3.75ns) | - | tWTR_S+ max (5nCK,3.75ns) | - | tWTR_S+ max (5nCK,3.75ns) | - | tWTR_S+ max (5nCK,3.75ns) | - | ns | 2, 29, 34 |
| delay from start of internal write transaction to internal read command for same bank group with both CRC and DM enabled | tWTR_L_CRC_DM | tWTR_L+ max (4nCK,3.75ns) | - | tWTR_L+ max (5nCK,3.75ns) | - | tWTR_L+ max (5nCK,3.75ns) | - | tWTR_L+ max (5nCK,3.75ns) | - | tWTR_L+ max (5nCK,3.75ns) | - | ns | 3,30, 34 |
| DLL locking time | tDLLK | 597 | - | 597 | - | 768 | - | 768 | - | 854 | - | nCK | |
| Mode Register Set command cycle time | tMRD | 8 | - | 8 | - | 8 | - | 8 | - | 8 | - | nCK | |
| Mode Register Set command update delay | tMOD | max(24nCK,15ns) | - | max(24nCK,15ns) | - | max(24nCK,15ns) | - | max(24nCK,15ns) | - | max(24nCK,15ns) | - | nCK | 50 |
| Multi-Purpose Register Recovery Time | tMPRR | 1 | - | 1 | - | 1 | - | 1 | - | 1 | - | nCK | 33 |
| Multi Purpose Register Write Recovery Time | tWR_MPR | tMOD (min) + AL + PL | - | tMOD (min) + AL + PL | - | tMOD (min) + AL + PL | - | tMOD (min) + AL + PL | - | tMOD (min) + AL + PL | - | nCK | |
| Auto precharge write recovery + precharge time | tDAL(min) | Programmed WR + roundup ( tRP / tCK(avg)) | | | | | | | | | | nCK | |
| DQ0 or DQL0 driven to 0 set-up time to first DQS rising edge | tPDA_S | 0.5 | - | 0.5 | - | 0.5 | - | 0.5 | - | 0.5 | - | UI | 45,47 |
| DQ0 or DQL0 driven to 0 hold time from last DQS fall-ing edge | tPDA_H | 0.5 | - | 0.5 | - | 0.5 | - | 0.5 | - | 0.5 | - | UI | 46,47 |
| **CS_n to Command Address Latency** | | | | | | | | | | | | | |
| CS_n to Command Address Latency | tCAL | max(3nCK, 3.748 ns) | - | max(3nCK, 3.748 ns) | - | max(3nCK, 3.748 ns) | - | max(3nCK, 3.748 ns) | - | max(3nCK, 3.748 ns) | - | nCK | |
| Mode Register Se commandt cycle time in CAL mode | tMRD_tCAL | tMOD+ tCAL | - | tMOD+ tCAL | - | tMOD+ tCAL | | tMOD+ tCAL | - | tMOD+ tCAL | - | nCK | |
| Mode Register Set update delay in CAL mode | tMOD_tCAL | tMOD+ tCAL | - | tMOD+ tCAL | - | tMOD+ tCAL | | tMOD+ tCAL | - | tMOD+ tCAL | - | nCK | |
| **DRAM Data Timing** | | | | | | | | | | | | | |
| DQS_t,DQS_c to DQ skew, per group, per access | tDQSQ | - | 0.16 | - | 0.16 | - | 0.16 | - | 0.17 | - | 0.18 | tCK(avg)/2 | 13,18,39,49 |
| DQ output hold per group, per access from DQS_t,DQS_c | tQH | 0.76 | - | 0.76 | - | 0.76 | - | 0.74 | - | 0.74 | - | tCK(avg)/2 | 13,17,18,39,49 |
| Data Valid Window per device: (tQH - tDQSQ) of each UI on a given DRAM | tDVWd | 0.63 | - | 0.63 | - | 0.64 | - | 0.64 | - | TBD | - | UI | 17,18,39,49 |
| Data Valid Window , per pin per UI : (tQH - tDQSQ) each UI on a pin of a given DRAM | tDVWp | 0.66 | - | 0.66 | - | 0.69 | - | 0.72 | - | 0.72 | - | UI | 17,18,39,49 |
| DQ low impedance time from CK_t, CK_c | tLZ(DQ) | -450 | 225 | -390 | 195 | -390 | 180 | -330 | 175 | -310 | 170 | ps | 39 |
| DQ high impedance time from CK_t, CK_c | tHZ(DQ) | - | 225 | - | 195 | - | 180 | - | 175 | - | 170 | ps | 39 |
| **Data Strobe Timing** | | | | | | | | | | | | | |
| DQS_t, DQS_c differential READ Pre-amble (1 clock preamble) | tRPRE | 0.9 | NOTE44 | 0.9 | NOTE44 | 0.9 | NOTE44 | 0.9 | NOTE 44 | 0.9 | NOTE 44 | tCK | 39,40 |
| DQS_t, DQS_c differential READ Pre-amble (2 clock preamble) | tRPRE2 | NA | NA | NA | NA | NA | NA | 1.8 | NOTE 44 | 1.8 | NOTE 44 | tCK | 39,41 |
| DQS_t, DQS_c differential READ Postamble | tRPST | 0.33 | NOTE 45 | 0.33 | NOTE 45 | 0.33 | NOTE 45 | 0.33 | NOTE 45 | 0.33 | NOTE 45 | tCK | 39 |

| Speed | | DDR4-1600 | | DDR4-1866 | | DDR4-2133 | | DDR4-2400 | | DDR4-2666 | | Units | NOTE |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Parameter | Symbol | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | | |
| DQS_t,DQS_c differential output high time | tQSH | 0.4 | - | 0.4 | - | 0.4 | - | 0.4 | - | 0.4 | - | tCK | 21,39 |
| DQS_t,DQS_c differential output low time | tQSL | 0.4 | - | 0.4 | - | 0.4 | - | 0.4 | - | 0.4 | - | tCK | 20,39 |
| DQS_t, DQS_c differential WRITE Pre-amble (1 clock preamble) | tWPRE | 0.9 | - | 0.9 | - | 0.9 | - | 0.9 | - | 0.9 | - | tCK | 42 |
| DQS_t, DQS_c differential WRITE Pre-amble (2 clock preamble) | tWPRE2 | NA | | NA | | NA | | 1.8 | - | 1.8 | - | tCK | 43 |
| DQS_t, DQS_c differential WRITE Postamble | tWPST | 0.33 | - | 0.33 | - | 0.33 | - | 0.33 | - | 0.33 | - | tCK | |
| DQS_t and DQS_c low-impedance time (Referenced from RL-1) | tLZ(DQS) | -450 | 225 | -390 | 195 | -360 | 180 | -330 | 175 | -310 | 170 | ps | 39 |
| DQS_t and DQS_c high-impedance time (Referenced from RL+BL/2) | tHZ(DQS) | - | 225 | - | 195 | - | 180 | - | 175 | - | 170 | ps | 39 |
| DQS_t, DQS_c differential input low pulse width | tDQSL | 0.46 | 0.54 | 0.46 | 0.54 | 0.46 | 0.54 | 0.46 | 0.54 | 0.46 | 0.54 | tCK | |
| DQS_t, DQS_c differential input high pulse width | tDQSH | 0.46 | 0.54 | 0.46 | 0.54 | 0.46 | 0.54 | 0.46 | 0.54 | 0.46 | 0.54 | tCK | |
| DQS_t, DQS_c rising edge to CK_t, CK_c rising edge (1 clock preamble) | tDQSS | -0.27 | 0.27 | -0.27 | 0.27 | -0.27 | 0.27 | -0.27 | 0.27 | -0.27 | 0.27 | tCK | 42 |
| DQS_t, DQS_c rising edge to CK_t, CK_c rising edge (2 clock preamble) | tDQSS2 | TBD | TBD | TBD | TBD | TBD | TBD | TBD | TBD | TBD | TBD | tCK | 43 |
| DQS_t, DQS_c falling edge setup time to CK_t, CK_c rising edge | tDSS | 0.18 | - | 0.18 | - | 0.18 | - | 0.18 | - | 0.18 | - | tCK | |
| DQS_t, DQS_c falling edge hold time from CK_t, CK_c rising edge | tDSH | 0.18 | - | 0.18 | - | 0.18 | - | 0.18 | - | 0.18 | - | tCK | |
| DQS_t, DQS_c rising edge output timing locatino from rising CK_t, CK_c with DLL On mode | tDQSCK (DLL On) | -225 | 225 | -195 | 195 | -180 | 180 | -175 | 175 | -170 | 170 | ps | 37,38,39 |
| DQS_t, DQS_c rising edge output variance window per DRAM | tDQSCKI (DLL On) | | 370 | | 330 | | 310 | | 290 | | 270 | ps | 37,38,39 |
| **MPSM Timing** | | | | | | | | | | | | | |
| Command path disable delay upon MPSM entry | tMPED | tMOD(min) + tCPDED(min) | - | tMOD(min) + tCPDED(min) | - | tMOD(min) + tCPDED(min) | - | tMOD(min) + tCPDED(min) | - | TBD | - | | |
| Valid clock requirement after MPSM entry | tCKMPE | tMOD(min) + tCPDED(min) | - | tMOD(min) + tCPDED(min) | - | tMOD(min) + tCPDED(min) | - | tMOD(min) + tCPDED(min) | - | TBD | - | | |
| Valid clock requirement before MPSM exit | tCKMPX | tCKSRX(min) | - | tCKSRX(min) | - | tCKSRX(min) | - | tCKSRX(min) | - | TBD | - | | |
| Exit MPSM to commands not requiring a locked DLL | tXMP | tXS(min) | - | tXS(min) | - | tXS(min) | - | tXS(min) | - | TBD | - | | |
| Exit MPSM to commands requiring a locked DLL | tXMPDLL | tXMP(min) + tXSDLL(min) | - | tXMP(min) + tXSDLL(min) | - | tXMP(min) + tXSDLL(min) | - | tXMP(min) + tXSDLL(min) | - | TBD | - | | |
| CS setup time to CKE | tMPX_S | tIS(min) + tIHL(min) | - | tIS(min) + tIHL(min) | - | tIS(min) + tIHL(min) | - | tIS(min) + tIHL(min) | - | TBD | - | | |
| **Calibration Timing** | | | | | | | | | | | | | |
| Power-up and RESET calibration time | tZQinit | 1024 | - | 1024 | - | 1024 | - | 1024 | - | 1024 | - | nCK | |
| Normal operation Full calibration time | tZQoper | 512 | - | 512 | - | 512 | - | 512 | - | 512 | - | nCK | |
| Normal operation Short calibration time | tZQCS | 128 | - | 128 | - | 128 | - | 128 | - | 128 | - | nCK | |
| **Reset/Self Refresh Timing** | | | | | | | | | | | | | |
| Exit Reset from CKE HIGH to a valid command | tXPR | max (5nCK,tRFC(min)+10ns) | - | max (5nCK,tRFC(min)+10ns) | - | max (5nCK,tRFC(min)+10ns) | - | max (5nCK,tRFC(min)+10ns) | - | max (5nCK,tRFC(min)+10ns) | - | nCK | |
| Exit Self Refresh to commands not requiring a locked DLL | tXS | tRFC(min)+10ns | - | tRFC(min)+10ns | - | tRFC(min)+10ns | - | tRFC(min)+10ns | - | tRFC(min)+10ns | - | nCK | |
| SRX to commands not requiring a locked DLL in Self Refresh ABORT | tXS_ABORT(min) | tRFC4(min)+10ns | - | tRFC4(min)+10ns | - | tRFC4(min)+10ns | - | tRFC4(min)+10ns | - | tRFC4(min)+10ns | - | nCK | |
| Exit Self Refresh to ZQCL,ZQCS and MRS (CL,CWL,WR,RTP and Gear Down) | tXS_FAST (min) | tRFC4(min)+10ns | - | tRFC4(min)+10ns | - | tRFC4(min)+10ns | - | tRFC4(min)+10ns | - | tRFC4(min)+10ns | - | nCK | |
| Exit Self Refresh to commands requiring a locked DLL | tXSDLL | tDLLK(min) | - | tDLLK(min) | - | tDLLK(min) | - | tDLLK(min) | - | tDLLK(min) | - | nCK | |
| Minimum CKE low width for Self refresh entry to exit timing | tCKESR | tCKE(min)+1nCK | - | tCKE(min)+1nCK | - | tCKE(min)+1nCK | - | tCKE(min)+1nCK | - | tCKE(min)+1nCK | - | nCK | |
| Minimum CKE low width for Self refresh entry to exit timing with CA Parity enabled | tCKESR_ PAR | tCKE(min)+ 1nCK+PL | - | tCKE(min)+ 1nCK+PL | - | tCKE(min)+ 1nCK+PL | - | tCKE(min)+ 1nCK+PL | - | tCKE(min)+ 1nCK+PL | - | nCK | |
| Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down Entry (PDE) | tCKSRE | max(5nCK,10ns) | - | max(5nCK,10ns) | - | max(5nCK,10ns) | - | max (5nCK,10ns) | - | max (5nCK,10ns) | - | nCK | |

| Speed | | DDR4-1600 | | DDR4-1866 | | DDR4-2133 | | DDR4-2400 | | DDR4-2666 | | Units | NOTE |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Parameter | Symbol | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | | |
| Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down when CA Parity is enabled | tCKSRE_PAR | max (5nCK,10 ns)+PL | - | max (5nCK,10 ns)+PL | - | max (5nCK,10 ns)+PL | - | max (5nCK,10 ns)+PL | - | max (5nCK,10 ns)+PL | - | nCK | |
| Valid Clock Requirement before Self Refresh Exit (SRX) or Power-Down Exit (PDX) or Reset Exit | tCKSRX | max(5nC K,10ns) | - | max(5nC K,10ns) | - | max(5nC K,10ns) | - | max (5nCK,10 ns) | - | max (5nCK,10 ns) | - | nCK | |
| **Power Down Timing** | | | | | | | | | | | | | |
| Exit Power Down with DLL on to any valid command;Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL | tXP | max (4nCK,6n s) | - | max (4nCK,6n s) | - | max (4nCK,6n s) | - | max (4nCK,6n s) | - | max (4nCK,6n s) | - | nCK | |
| CKE minimum pulse width | tCKE | max (3nCK, 5ns) | - | max (3nCK, 5ns) | - | max (3nCK, 5ns) | - | max (3nCK, 5ns) | - | max (3nCK, 5ns) | - | nCK | 31,32 |
| Command pass disable delay | tCPDED | 4 | - | 4 | - | 4 | - | 4 | - | 4 | - | nCK | |
| Power Down Entry to Exit Timing | tPD | tCKE(min ) | 9*tREFI | tCKE(min ) | 9*tREFI | tCKE(min ) | 9*tREFI | tCKE(min ) | 9*tREFI | tCKE(min ) | 9*tREFI | nCK | 6 |
| Timing of ACT command to Power Down entry | tACTPDEN | 1 | - | 1 | - | 2 | - | 2 | - | 2 | - | nCK | 7 |
| Timing of PRE or PREA command to Power Down entry | tPRPDEN | 1 | - | 1 | - | 2 | - | 2 | - | 2 | - | nCK | 7 |
| Timing of RD/RDA command to Power Down entry | tRDPDEN | RL+4+1 | - | RL+4+1 | - | RL+4+1 | - | RL+4+1 | - | RL+4+1 | - | nCK | |
| Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BC4OTF) | tWRPDEN | WL+4+(t WR/ tCK(avg)) | - | WL+4+(t WR/ tCK(avg)) | - | WL+4+(t WR/ tCK(avg)) | - | WL+4+(t WR/ tCK(avg)) | - | WL+4+(t WR/ tCK(avg)) | - | nCK | 4 |
| Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BC4OTF) | tWRAPDEN | WL+4+W R+1 | - | WL+4+W R+1 | - | WL+4+W R+1 | - | WL+4+W R+1 | - | WL+4+W R+1 | - | nCK | 5 |
| Timing of WR command to Power Down entry (BC4MRS) | tWRP-BC4DEN | WL+2+(t WR/ tCK(avg)) | - | WL+2+(t WR/ tCK(avg)) | - | WL+2+(t WR/ tCK(avg)) | - | WL+2+(t WR/ tCK(avg)) | - | WL+2+(t WR/ tCK(avg)) | - | nCK | 4 |
| Timing of WRA command to Power Down entry (BC4MRS) | tWRAP-BC4DEN | WL+2+W R+1 | - | WL+2+W R+1 | - | WL+2+W R+1 | - | WL+2+W R+1 | - | WL+2+W R+1 | - | nCK | 5 |
| Timing of REF command to Power Down entry | tREFPDEN | 1 | - | 1 | - | 2 | - | 2 | - | 2 | - | nCK | 7 |
| Timing of MRS command to Power Down entry | tMRSPDEN | tMOD(mi n) | - | tMOD(mi n) | - | tMOD(mi n) | - | tMOD(mi n) | - | tMOD(mi n) | - | nCK | |
| **PDA Timing** | | | | | | | | | | | | | |
| Mode Register Set command cycle time in PDA mode | tMRD_PDA | max(16n CK,10ns) | - | max(16n CK,10ns) | - | max(16n CK,10ns) | - | max(16n CK,10ns) | - | max(16n CK,10ns) | - | nCK | |
| Mode Register Set command update delay in PDA mode | tMOD_PDA | tMOD | | tMOD | | tMOD | | tMOD | | tMOD | | nCK | |
| **ODT Timing** | | | | | | | | | | | | | |
| Asynchronous RTT turn-on delay (Power-Down with DLL frozen) | tAONAS | 1.0 | 9.0 | 1.0 | 9.0 | 1.0 | 9.0 | 1.0 | 9.0 | 1.0 | 9.0 | ns | |
| Asynchronous RTT turn-off delay (Power-Down with DLL frozen) | tAOFAS | 1.0 | 9.0 | 1.0 | 9.0 | 1.0 | 9.0 | 1.0 | 9.0 | 1.0 | 9.0 | ns | |
| RTT dynamic change skew | tADC | 0.3 | 0.7 | 0.3 | 0.7 | 0.3 | 0.7 | 0.3 | 0.7 | 0.3 | 0.7 | tCK(avg) | |
| **Write Leveling Timing** | | | | | | | | | | | | | |
| First DQS_t/DQS_n rising edge after write leveling mode is programmed | tWLMRD | 40 | - | 40 | - | 40 | - | 40 | - | 40 | - | nCK | 12 |
| DQS_t/DQS_n delay after write leveling mode is programmed | tWLDQSEN | 25 | - | 25 | - | 25 | - | 25 | - | 25 | - | nCK | 12 |
| Write leveling setup time from rising CK_t, CK_c crossing to rising DQS_t/DQS_n crossing | tWLS | 0.13 | - | 0.13 | - | 0.13 | - | 0.13 | - | 0.13 | - | tCK(avg) | |
| Write leveling hold time from rising DQS_t/ DQS_n crossing to rising CK_t, CK_ crossing | tWLH | 0.13 | - | 0.13 | - | 0.13 | - | 0.13 | - | 0.13 | - | tCK(avg) | |
| Write leveling output delay | tWLO | 0 | 9.5 | 0 | 9.5 | 0 | 9.5 | 0 | 9.5 | 0 | 9.5 | ns | |
| Write leveling output error | tWLOE | 0 | 2 | 0 | 2 | 0 | 2 | 0 | 2 | 0 | 2 | ns | |
| **CA Parity Timing** | | | | | | | | | | | | | |
| Commands not guaranteed to be executed during this time | tPAR_UNKNOWN | - | PL | - | PL | - | PL | - | PL | - | PL | nCK | |
| Delay from errant command to ALERT_n assertion | tPAR_ALERT_ON | - | PL+6ns | - | PL+6ns | - | PL+6ns | - | PL+6ns | - | PL+6ns | nCK | |
| Pulse width of ALERT_n signal when asserted | tPAR_ALERT_PW | 48 | 96 | 56 | 112 | 64 | 128 | 72 | 144 | 80 | 160 | nCK | |
| Time from when Alert is asserted till controller must start providing DES commands in Persistent CA parity mode | tPAR_ALERT_RSP | - | 43 | - | 50 | - | 57 | - | 64 | | 71 | nCK | |
| Parity Latency | PL | 4 | | 4 | | 4 | | 5 | | 5 | | nCK | |

| Speed | | DDR4-1600 | | DDR4-1866 | | DDR4-2133 | | DDR4-2400 | | DDR4-2666 | | Units | NOTE |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Parameter | Symbol | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | | |
| **CRC Error Reporting** | | | | | | | | | | | | | |
| CRC error to ALERT_n latency | tCRC_ALERT | 3 | 13 | 3 | 13 | 3 | 13 | 3 | 13 | 3 | 13 | ns | |
| CRC ALERT_n pulse width | CRC_ALERT_PW | 6 | 10 | 6 | 10 | 6 | 10 | 6 | 10 | 6 | 10 | nCK | |
| **Geardown timing** | | | | | | | | | | | | | |
| Exit RESET from CKE HIGH to a valid MRS geardown (T2/Reset) | tXPR_GEAR | - | - | - | - | - | - | - | - | TBD | | | |
| CKE High Assert to Gear Down Enable time(T2/CKE) | tXS_GEAR | - | - | - | - | - | - | - | - | TBD | | | |
| MRS command to Sync pulse time(T3) | tSYNC_GEAR | - | - | - | - | - | - | - | - | TBD | - | | 27 |
| Sync pulse to First valid command(T4) | tCMD_GEAR | - | - | - | - | - | - | - | - | TBD | | | 27 |
| Geardown setup time | tGEAR_setup | - | - | - | - | - | - | - | - | 2 | - | nCK | |
| Geardown hold time | tGEAR_hold | - | - | - | - | - | - | - | - | 2 | - | nCK | |
| **tREFI** | | | | | | | | | | | | | |
| tRFC1 (min) | 2Gb | 160 | - | 160 | - | 160 | - | 160 | - | 160 | - | ns | 34 |
| | 4Gb | 260 | - | 260 | - | 260 | - | 260 | - | 260 | - | ns | 34 |
| | 8Gb | 350 | - | 350 | - | 350 | - | 350 | - | 350 | - | ns | 34 |
| | 16Gb | 550 | - | 550 | - | 550 | - | 550 | - | 550 | - | ns | 34 |
| tRFC2 (min) | 2Gb | 110 | - | 110 | - | 110 | - | 110 | - | 110 | - | ns | 34 |
| | 4Gb | 160 | - | 160 | - | 160 | - | 160 | - | 160 | - | ns | 34 |
| | 8Gb | 260 | - | 260 | - | 260 | - | 260 | - | 260 | - | ns | 34 |
| | 16Gb | 350 | - | 350 | - | 350 | - | 350 | - | 350 | - | ns | 34 |
| tRFC4 (min) | 2Gb | 90 | - | 90 | - | 90 | - | 90 | - | 90 | - | ns | 34 |
| | 4Gb | 110 | - | 110 | - | 110 | - | 110 | - | 110 | - | ns | 34 |
| | 8Gb | 160 | - | 160 | - | 160 | - | 160 | - | 160 | - | ns | 34 |
| | 16Gb | 260 | - | 260 | - | 260 | - | 260 | - | 260 | - | ns | 34 |

**NOTE :**

1. Start of internal write transaction is defined as follows :
   For BL8 (Fixed by MRS and on-the-fly) : Rising clock edge 4 clock cycles after WL.
   For BC4 (on-the-fly) : Rising clock edge 4 clock cycles after WL.
   For BC4 (fixed by MRS) : Rising clock edge 2 clock cycles after WL.
2. A separate timing parameter will cover the delay from write to read when CRC and DM are simultaneously enabled
3. Commands requiring a locked DLL are: READ (and RAP) and synchronous ODT commands.
4. tWR is defined in ns, for calculation of tWRPDEN it is necessary to round up tWR/tCK to the next integer.
5. WR in clock cycles as programmed in MR0.
6. tREFI depends on TOPER.
7. CKE is allowed to be registered low while operations such as row activation, precharge, autoprecharge or refresh are in progress, but power-down IDD spec will not be applied until finishing those operations.
8. For these parameters, the DDR4 SDRAM device supports tnPARAM[nCK]=RU{tPARAM[ns]/tCK(avg)[ns]}, which is in clock cycles assuming all input clock jitter specifications are satisfied
9. When CRC and DM are both enabled, tWR_CRC_DM is used in place of tWR.
10. When CRC and DM are both enabled tWTR_S_CRC_DM is used in place of tWTR_S.
11. When CRC and DM are both enabled tWTR_L_CRC_DM is used in place of tWTR_L.
12. The max values are system dependent.
13. DQ to DQS total timing per group where the total includes the sum of deterministic and random timing terms for a specified BER. BER spec and measurement method are tbd.
14. The deterministic component of the total timing. Measurement method tbd.
15. DQ to DQ static offset relative to strobe per group. Measurement method tbd.
16. This parameter will be characterized and guaranteed by design.
17. When the device is operated with the input clock jitter, this parameter needs to be derated by the actual tjit(per)_total of the input clock. (output deratings are relative to the SDRAM input clock). Example tbd.
18. DRAM DBI mode is off.
19. DRAM DBI mode is enabled. Applicable to x8 and x16 DRAM only.
20. tQSL describes the instantaneous differential output low pulse width on DQS_t - DQS_c, as measured from on falling edge to the next consecutive rising edge
21. tQSH describes the instantaneous differential output high pulse width on DQS_t - DQS_c, as measured from on falling edge to the next consecutive rising edge
22. There is no maximum cycle time limit besides the need to satisfy the refresh interval tREFI
23. tCH(abs) is the absolute instantaneous clock high pulse width, as measured from one rising edge to the following falling edge
24. tCL(abs) is the absolute instantaneous clock low pulse width, as measured from one falling edge to the following rising edge
25. Total jitter includes the sum of deterministic and random jitter terms for a specified BER. BER target and measurement method are tbd.
26. The deterministic jitter component out of the total jitter. This parameter is characterized and gauranteed by design.
27. This parameter has to be even number of clocks
28. When CRC and DM are both enabled, tWR_CRC_DM is used in place of tWR.
29. When CRC and DM are both enabled tWTR_S_CRC_DM is used in place of tWTR_S.
30. When CRC and DM are both enabled tWTR_L_CRC_DM is used in place of tWTR_L.
31. After CKE is registered LOW, CKE signal level shall be maintained below VILDC for tCKE specification ( Low pulse width ).
32. After CKE is registered HIGH, CKE signal level shall be maintained above VIHDC for tCKE specification ( HIGH pulse width ).
33. Defined between end of MPR read burst and MRS which reloads MPR or disables MPR function.
34. Parameters apply from tCK(avg)min to tCK(avg)max at all standard JEDEC clock period values as stated in the Speed Bin Tables.
35. This parameter must keep consistency with Speed-Bin Tables .
36. DDR4-1600 AC timing apply if DRAM operates at lower than 1600 MT/s data rate.
    UI=tCK(avg).min/2
37. applied when DRAM is in DLL ON mode.
38. Assume no jitter on input clock signals to the DRAM
39. Value is only valid for RZQ/7 RONNOM = 34 ohms
40. 1tCK toggle mode with setting MR4:A11 to 0
41. 2tCK toggle mode with setting MR4:A11 to 1, which is valid for DDR4-2400/2666/3200 speed grade.
42. 1tCK mode with setting MR4:A12 to 0
43. 2tCK mode with setting MR4:A12 to 1, which is valid for DDR4-2400/2666/3200 speed grade.
44. The maximum read preamble is bounded by tLZ(DQS)min on the left side and tDQSCK(max) on the right side.
45. DQ falling signal middle-point of transferring from High to Low to first rising edge of DQS diff-signal cross-point
46. last falling edge of DQS diff-signal cross-point to DQ rising signal middle-point of transferring from Low to High
47. VrefDQ value must be set to either its midpoint or Vcent_DQ(midpoint) in order to capture DQ0 or DQL0 low level for entering PDA mode.
48. The maximum read postamble is bound by tDQSCK(min) plus tQSH(min) on the left side and tHZ(DQS)max on the right side.
49. Reference level of DQ output signal is specified with a midpoint as a widest part of Output signal eye which should be approximately 0.7 * VDDQ as a center level of the static single-ended output peak-to-peak swing with a driver impedance of 34 ohms and an effective test load of 50 ohms to VTT = VDDQ .
50. For MR7 commands, the minimum delay to a subsequent non-MRS command is 5nCK.

## 14.5 Rounding Algorithms

Software algorithms for calculation of timing parameters are subject to rounding errors from many sources. For example, a system may use a memory clock with a nominal frequency of 933.33... MHz, or a clock period of 1.0714... ns. Similarly, a system with a memory clock frequency of 1066.66... MHz yields mathematically a clock period of 0.9375... ns. In most cases, it is impossible to express all digits after the decimal point exactly, and rounding must be done because the DDR4 SDRAM specification establishes a minimum granularity for timing parameters of 1 ps.

Rules for rounding must be defined to allow optimization of device performance without violating device parameters. These algorithms rely on results that are within correction factors on device testing and specification to avoid losing performance due to rounding errors.

These rules are:

- Clock periods such as tCKAVGmin are defined to 1 ps of accuracy; for example, 0.9375... ns is defined as 937 ps and 1.0714... ns is defined as 1071 ps.
- Using real math, parameters like tAAmin, tRCDmin, etc. which are programmed in systems in numbers of clocks (nCK) but expressed in units of time (in ns) are divided by the clock period (in ns) yielding a unitless ratio, a correction factor of 2.5% is subtracted, then the result is set to the next higher integer number of clocks:

nCK = ceiling [ (parameter_in_ns / application_tCK_in_ns) - 0.025 ]

- Alternatively, programmers may prefer to use integer math instead of real math by expressing timing in ps, scaling the desired parameter value by 1000, dividing by the application clock period, adding an inverse correction factor of 97.4%, dividing the result by 1000, then truncating down to the next lower integer value:

nCK = truncate [ {(parameter_in_ps x 1000) / (application_tCK_in_ps) + 974} / 1000 ]

- Either algorithm yields identical results

## 14.6 The DQ Input Receiver Compliance Mask for Voltage and Timing

The DQ input receiver compliance mask for voltage and timing is shown in the figure below. The receiver mask (Rx Mask) defines area the input signal must not encroach in order for the DRAM input receiver to be expected to be able to successfully capture a valid input signal with BER of 1e-16; any input signal encroaching within the Rx Mask is subject to being invalid data. The Rx Mask is the receiver property for each DQ input pin and it is not the valid data-eye..

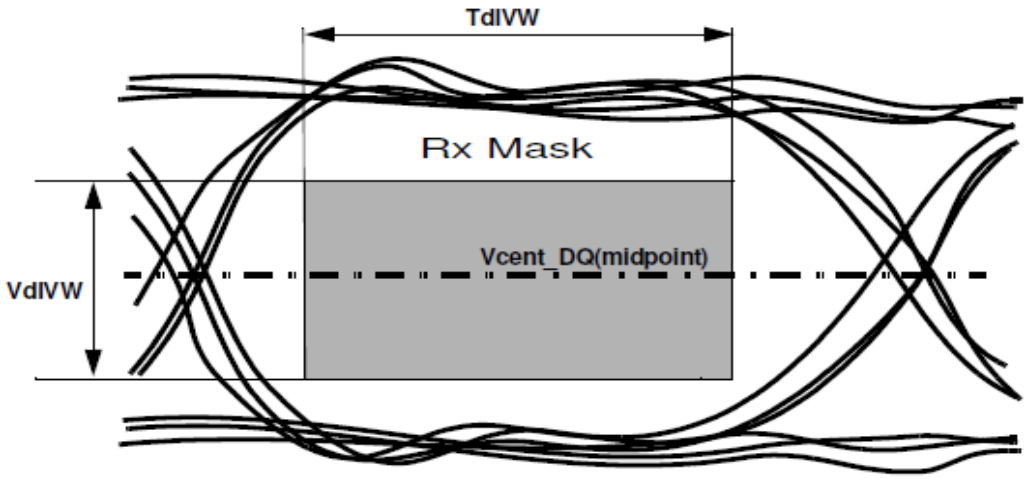



**Figure 24. DQ Receiver(Rx) compliance mask**

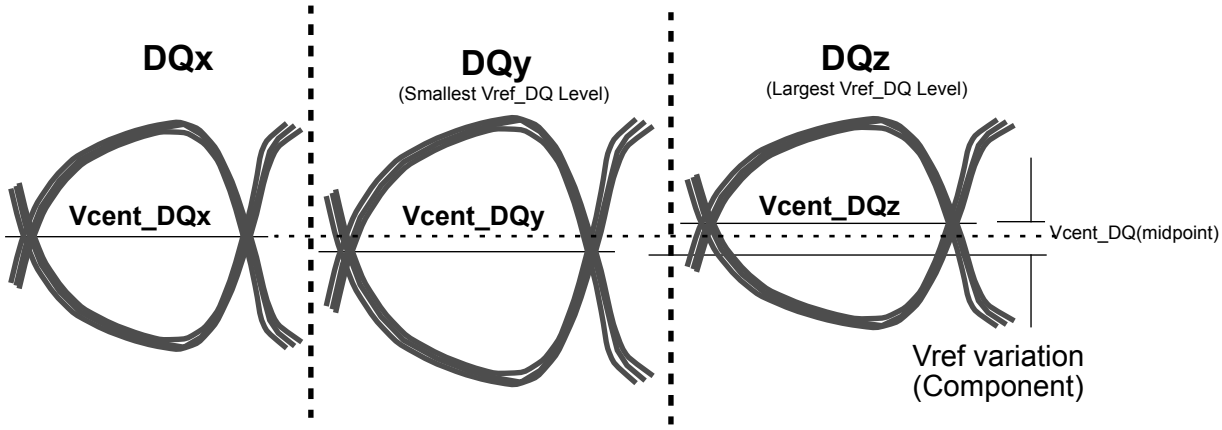
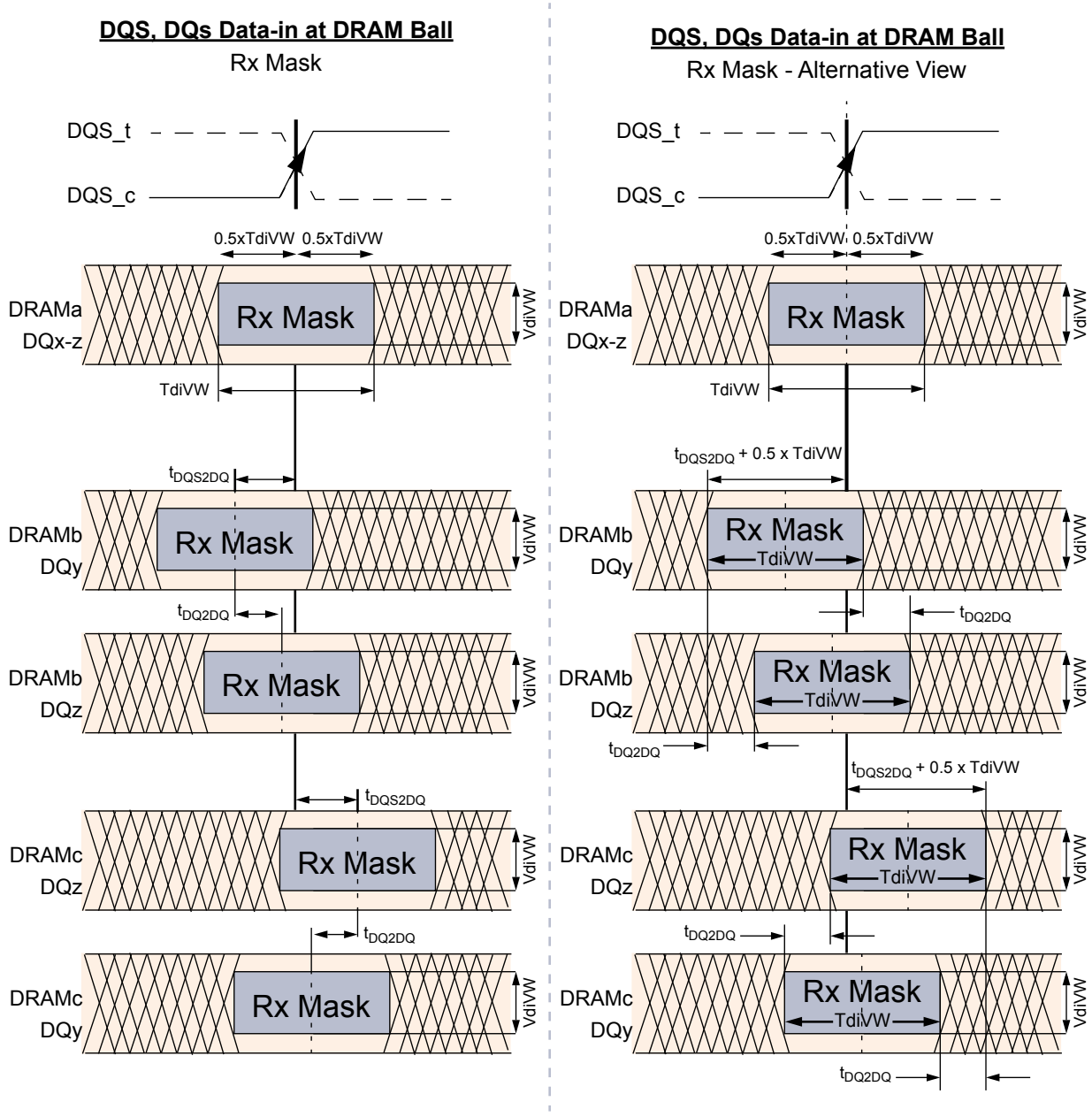



**Figure 25. Vcent_DQ Variation to Vcent_DQ(midpoint)**

The Vref_DQ voltage is an internal reference voltage level that shall be set to the properly trained setting, which is generally Vcent_DQ(midpoint), in order to have valid Rx Mask values.

Vcent_DQ is defined as the midpoint between the largest Vref_DQ voltage level and the smallest Vref_DQ voltage level across all DQ pins for a given DDR4 DRAM component. Each DQ pin Vref level is defined by the center, i.e. widest opening, of the cumulative data input eye as depicted in Figure 25.This clarifies that any DDR4 DRAM component level variation must be accounted for within the DDR4 DRAM Rx mask.The component level Vref will be set by the system to account for Ron and ODT settings.




NOTE : DQx represents an optimally centered mask.
DQy represents earliest valid mask.
DQz represents latest valid mask.

NOTE : DRAMa represents a DRAM without any DQS/DQ skews.
DRAMb represents a DRAM with early skews (negative $t_{DQS2DQ}$).
DRAMc represents a DRAM with delayed skews (positive $t_{DQS2DQ}$).

NOTE : Figures show skew allowed between DRAM to DRAM and DQ to DQ for a DRAM. Signals assume data centered aligned at DRAM Latch.
TdiPW is not shown; composite data-eyes shown would violate TdiPW.
VCENT DQ(midpoint) is not shown but is assummed to be midpoint of VdiVW..

**Figure 26. DQS to DQ and DQ to DQ Timings at DRAM Balls**

All of the timing terms in Figure 26 are measured at the VdIVW levels centered around Vcent_DQ(midpoint) and are referenced to the DQS_t/DQS_c center aligned to the DQ per pin.

The rising edge slew rates are defined by srr1 and srr2. The slew rate measurement points for a rising edge are shown in Figure 27 below: A low to high transition tr1 is measured from 0.5*VdiVW(max) below Vcent_DQ(midpoint) to the last transition through 0.5*VdiVW(max) above Vcent_DQ(midpoint) while tr2 is measured from the last transition through 0.5*VdiVW(max) above Vcent_DQ(midpoint) to the first transition through the 0.5*VIHL_AC(min) above Vcent_DQ(midpoint).

Rising edge slew rate equations:

srr1 = VdIVW(max) / tr1

srr2 = (VIHL_AC(min) – VdIVW(max)) / (2*tr2)

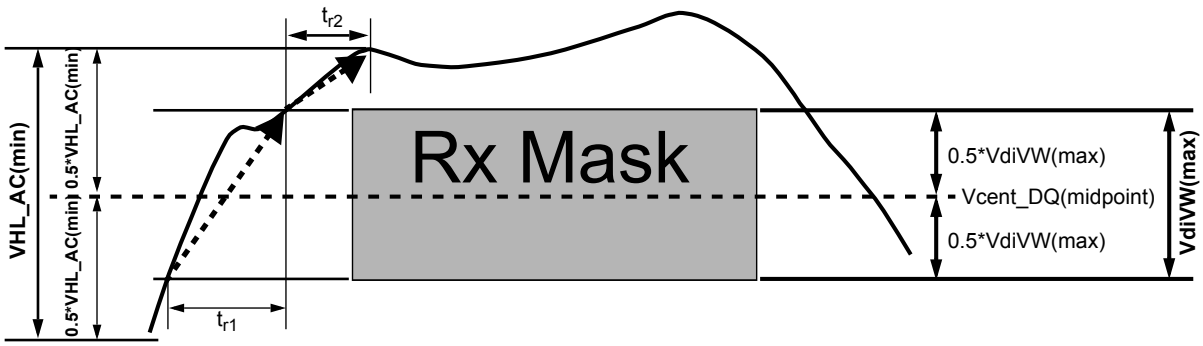



**Figure 27. Slew Rate Conditions For Rising Transition**

The falling edge slew rates are defined by srf1 and srf2. The slew rate measurement points for a falling edge are shown in Figure 28 below: A high to low transition tf1 is measured from 0.5*VdiVW(max) above Vcent_DQ(midpoint) to the last transition through 0.5*VdiVW(max) below Vcent_DQ(midpoint) while tf2 is measured from the last transition through 0.5*VdiVW(max) below Vcent_DQ(midpoint) to the first transition through the 0.5*VIHL_AC(min) below Vcent_DQ(pin mid).

Falling edge slew rate equations:

srf1 = VdIVW(max) / tf1

srf2 = (VIHL_AC(min) – VdIVW(max)) / (2*tf2)

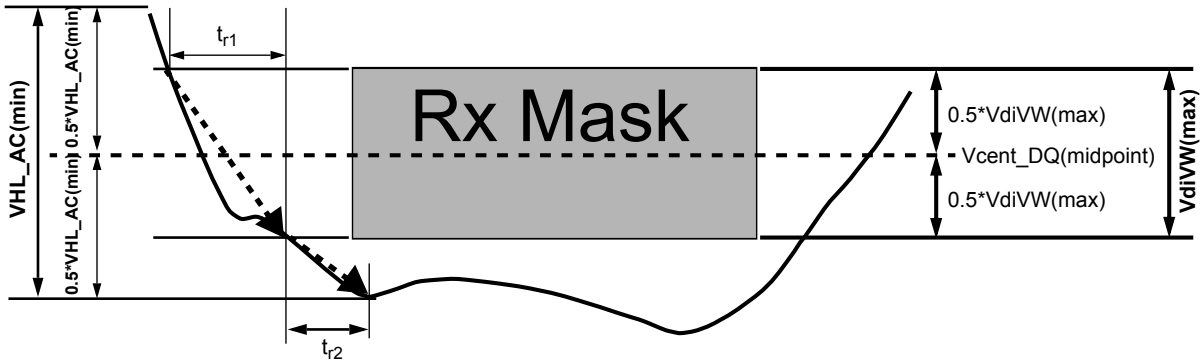



**Figure 28. Slew Rate Conditions For Falling Transition**

**[ Table 54 ] DRAM DQs In Receive Mode;** * UI=tck(avg)min/2

| Symbol | Parameter | 1600/1866/2133 | | 2400 | | 2666 | | Unit | NOTE |
|---|---|---|---|---|---|---|---|---|---|
| | | min | max | min | max | min | max | | |
| VdIVW | Rx Mask voltage - pk-pk | - | 136 | - | 130 | - | 120 | mV | 1,2,10 |
| TdIVW | Rx timing window | - | 0.2 | - | 0.2 | - | 0.22 | UI* | 1,2,10 |
| VIHL_AC | DQ AC input swing pk-pk | 186 | - | 160 | - | 150 | - | mV | 3,4,10 |
| TdIPW | DQ input pulse width | 0.58 | | 0.58 | | 0.58 | - | UI* | 5,10 |
| tDQS2DQ | Rx Mask DQS to DQ offset | -0.17 | 0.17 | -0.17 | 0.17 | -0.19 | 0.19 | UI* | 6, 10 |
| tDQ2DQ | Rx Mask DQ to DQ offset | - | tbd | - | tbd | | tbd | UI* | 7 |
| srr1, srf1 | Input Slew Rate over VdIVW if tCK >= 0.935ns | 1.0 | 9 | 1.0 | 9 | 1.0 | tbd | V/ns | 8,10 |
| | Input Slew Rate over VdIVW if 0.935ns > tCK >= 0.625ns | - | - | 1.25 | 9 | 1 | tbd | V/ns | 8,10 |
| srr2 | Rising Input Slew Rate over 1/2 VIHL_AC | 0.2*srr1 | 9 | 0.2*srr1 | 9 | 0.2*srr1 | tbd | V/ns | 9,10 |
| srf2 | Falling Input Slew Rate over 1/2 VIHL_AC | 0.2*srf1 | 9 | 0.2*srf1 | 9 | 0.2*srr1 | tbd | V/ns | 9,10 |

**NOTE :**

1. Data Rx mask voltage and timing total input valid window where VdIVW is centered around Vcent_DQ( midpoint) after VrefDQ training is completed. The data Rx mask is applied per bit and should include voltage and temperature drift terms. The input buffer design specification is to achieve at least a BER = e-16 when the RxMask is not violated. The BER will be characterized and extrapolated if necessary using a dual dirac method from a higher BER(tbd).
2. Defined over the DQ internal Vref range 1.
3. See Overshoot and Undershoot Specification.
4. DQ input pulse signal swing into the receiver must meet or exceed VIHL AC(min). . VIHL_AC(min) is to be achieved on an UI basis when a rising and falling edge occur in the same UI, i.e. a valid TdiPW.
5. DQ minimum input pulse width defined at the Vcent_DQ( midpoint).
6. DQS to DQ offset is skew between DQS and DQs within a nibble (x4) or word (x8, x16) at the DDR4 SDRAM balls over process, voltage, and temperature.
7. DQ to DQ offset is skew between DQs within a nibble (x4) or word (x8, x16) at the DDR4 SDRAM balls for a given component over process, voltage, and temperature.
8. Input slew rate over VdIVW Mask centered at Vcent_DQ( midpoint). Slowest DQ slew rate to fastest DQ slew rate per transition edge must be within 1.7 V/ns of each other.
9. Input slew rate between VdIVW Mask edge and VIHL_AC(min) points.
10. All Rx Mask specifications must be satisfied for each UI. For example, if the minimum input pulse width is violated when satisfying TdiVW(min), VdiVW(max), and minimum slew rate limits, then either TdiVW(min) or minimum slew rates would have to be increased to the point where the minimum input pulse width would no longer be violated.

## 14.7 DDR4 Function Matrix

DDR4 SDRAM has several features supported by ORG and also by Speed. The following Table is the summary of the features.

**[ Table 55 ] Function Matrix (By ORG. V:Supported, Blank:Not supported)**

| Functions | x4 | x8 | x16 | NOTE |
|---|---|---|---|---|
| Write Leveling | V | V | V | |
| Temperature controlled Refresh | V | V | V | |
| Low Power Auto Self Refresh | V | V | V | |
| Fine Granularity Refresh | V | V | V | |
| Multi Purpose Register | V | V | V | |
| Data Mask | | V | V | |
| Data Bus Inversion | | V | V | |
| TDQS | | V | | |
| ZQ calibration | V | V | V | |
| DQ Vref Training | V | V | V | |
| Per DRAM Addressability | V | V | V | |
| Mode Register Readout | V | V | V | |
| CAL | V | V | V | |
| WRITE CRC | V | V | V | |
| CA Parity | V | V | V | |
| Control Gear Down Mode | V | V | V | |
| Programmable Preamble | V | V | V | |
| Maximum Power Down Mode | V | V | | |
| Boundary Scan Mode | | | V | |
| Additive Latency | V | V | | |
| 3DS | V | V | | |

**[ Table 56 ] Function Matrix (By Speed. V:Supported, Blank:Not supported)**

| Functions | DLL Off mode | DLL On mode | | | NOTE |
|---|---|---|---|---|---|
| | equal or slower than 250Mbps | 1600/1866/2133 Mbps | 2400Mbps | 2666Mbps | |
| Write Leveling | V | V | V | V | |
| Temperature controlled Refresh | V | V | V | V | |
| Low Power Auto Self Refresh | V | V | V | V | |
| Fine Granularity Refresh | V | V | V | V | |
| Multi Purpose Register | V | V | V | V | |
| Data Mask | V | V | V | V | |
| Data Bus Inversion | V | V | V | V | |
| TDQS | | V | V | V | |
| ZQ calibration | V | V | V | V | |
| DQ Vref Training | V | V | V | V | |
| Per DRAM Addressability | | V | V | V | |
| Mode Register Readout | V | V | V | V | |
| CAL | | V | V | V | |
| WRITE CRC | | V | V | V | |
| CA Parity | | V | V | V | |
| Control Gear Down Mode | | | | V | |
| Programmable Preamble (= 2tCK) | | | V | V | |
| Maximum Power Down Mode | | V | V | V | |
| Boundary Scan Mode | V | V | V | V | |
| 3DS | V | V | V | V | |